SERVICE MANUAL FOR

M230

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M230 N/B Maintenance

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineering specification for M230 portable notebook computer system. The M230 notebook computer is a new mainstream high performance thin and light notebook in the MiTAC notebook family.

1.1.2 System Overview – Marketing Requirement

The new M230 is ruggedized notebook, high-portability industrial computer. It can be used in the vehicle field and office. The notebook computer also can connect with a docking to extend the capability of I/O devices.

The M230 will support the Intel Mobile Pentium M based on 65 nm technology – Yonah 1.66 GHz processor or 1.5 GHz (option) processor via the 479-ball Micro-FCBGA packages and an operating Front Side Bus speed of 667 MHz.

The Intel 945GM north bridge chipset supports host system bus at 667 MHz, 2 slots of DDR2 SODIMM (400/533 MHz) 256 MB to 2 GB total, internal video controller support RGB, TV-out, SDVO and LVDS video interfaces and hub interface to south bridge ICH7-M.

The Intel 82801GBM (ICH7-M) south bridge supports PCI 2.3 interface, integrated IDE (PATA) controller, integrated Serial ATA (SATA) controller, integrated USB hub 2.0 up to 8 ports, integrated LAN 10/100 Mbit/s, integrated Intel high definition controller (Azalia), LPC interface, SMBus 2.0 interface, FWH interface, Real Time

Clock (RTC), IRQ controller and advance programmable interrupt controller (APIC) support.

On PCI Bus interface exist PCI1520 card-bus controller and TSB82AA2 1394B controller that supports PC cards and 1394B device separately, Wireless LAN on mini PCIE interface and X-BAY radio interface.

On LPC interface exist super I/O that is SIO10N268. It provides four serial ports and one parallel port. The LPC will connect the Keyboard embedded controller H8S/2140 and flash memory for BIOS.

There are two SMBus interfaces, one is connected from ICH7-M and operating under master mode, the second is multi-master Bus and connected from H8S/2140. The Master provides interface to synthesizer and to memory identification. The multi-master channel used for thermal sensor controller (SMBus from LCD interface and SMBus from Docking).

A CODEC (ALC260) with TI audio amplifier stereo analog audio to internal speakers, audio jack and docking. Digital audio-PDIF standard also provided to audio jack and to docking.

System also provides LEDs to display system status, such as power on, battery state, HDD, Num Lock, Caps Lock and Scroll Lock.

The system also provides a port to expand docking capability. Input/Output (I/O) ports can include parallel port, serial port, VGA port, USB, line out, video input.

The system also provides DVD-ROM, Bluetooth, GPS, X-BAY radios.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 2000 and Windows XP to take full advantage of the hardware capabilities.

Detailed specs as follow.

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Features	
CPU	Standard: Intel Yonah processor LV dual core 1.66 GHz in µ-FCBGA package Intel Yonah processor LV dual core 1.5 GHz in µ-FCBGA package
	CPU thermal ceiling: 15 W
	FSB 667 MHz
Core Logic	Intel 945GM chipset (Calistoga) + ICH7-M (PCI Express x 6 channels)
L2 Cache	on-die 2 MB
System BIOS	1 MB flash EPROM
	Includes system BIOS (Phoenix solution, Kernel core version), VGA BIOS, plug & play, ACPI2.0 capability
	Boot from IDE & SATA devices, USB CD-ROM, USB FDD
	Suspend to DRAM/HDD PC2001 compliance
Memory	Standard: 256 MB
	Options: 512 MB/1 GB/2 GB (Max system memory of 2 GB in 2 slots)
	Supports 400/533 MHz DDR2 devices
	2 DDR2 SO-DIMM (200-pin)
VGA Controller	- Integrated in 945GM chipset, Intel GMA950 graphic controller
	- Optional ATI M54-CSP VGA controller with 128 MB memory
	- Dual view function/LCD/CRT simultaneous display capability
Display	- 14.1" TFT XGA (1024 x 768) SPWG type 14.1" LCD
	- 15.0" TFT SXGA+ (1400 x 1050) SPWG type 15.0" LCD (Optional)
	Factory optional touch screen
	Factory option Hi-Contrast solution for 14" panel only
Structure	3-spindle
Video Memory	Shared system memory 64 MB
HDD	- Standard: Serial ATA 60 GB; up to 120 GB (5400 or 7200 rpm)
	- Factory optional HDD heater for low temperature (-20 C~55 C) support
	- Optional low temperature 20 GB HDD without HDD heater

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HDD	- Built-in design to support operating mode free drop from 0 to 3 feet heigh
	1~3 feet: Protected by G-sensor
	0~1 foot: Protected by special construction resistance design
CD-ROM Bay	Easy swappable bay for CD-ROM/COMBO Drive/DVD dual recorder/2nd battery
Keyboard	- Water-proof membrane keyboard
	- Factory optional water-proof rubber keyboard
	- Factory optional back-light rubber keyboard
Pointing Device	A sensitive control touch pad: capacitance type (Optional water-proof: resistance type)
PCMCIA	- Type II x 2 - Card Bus support
	- Type II x 1 and built-in smart card reader x 1 (optional)
Audio	Azalia 32 bits 192 KHz/AC97' 2.3 Audio digital controllerBuild-in Stereo 2 W speakers
I/O Ports	- Serial port x 1
	- USB 2.0 x 2 (USB power support maximum 1 A per port)
	- IrDA FIR x 1
	- DC input x 1
	- Docking Port (POGO pin, hot docking) compatible with M220
	- CRT port x 1
	- 1394B port x 1 (Optional: PS2 port x 1)
	- Parallel port x 1
	- RJ-45 x 1
	- RJ-11 x 1
	- Microphone-in x 1
	- Line-out x 1
Communication	- Integrated 10/100/1000 base-T Ethernet with TPM security function
	- Integrated 56 kbps Modem
	- Integrated Wireless LAN (802.11 a/b/g) with antenna
	- Factory optional GPS module with antenna
	- Factory optional wireless module for GSM GPRS/CDMA with antenna

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Communication	- Factory optional Bluetooth with antenna
	- No any interface between 4 antennas in the same time
Cooling	No fan
Battery	- Main battery supports over 5 hours
	- Second battery supports over 2 hours (Based on system without M54 VGA controller)
AC Adaptor	- 90 Watts universal or above, auto sensing/switching, fully support all the functions
	- Input: 100-240 V, 50/60 Hz AC
Dimensions	- 328 x 272.1 x 46 mm for M230-4 (14.1")
	- 338 x 286 x 46 mm for M230-5 (15") -Same dimension as M220
Weight	x1 (Front side)
Software	USB2.0, right side x 2, rear side x 2
Environmental Standard (Main System)	
Temperature	IEC 68-2-1,2,14 / MIL-STD-810F, Method 501.4, 502.4
	Operating: 0°C to 55 ° C (standard)-W/O battery pack > 50 ° C
	-20°C to 60 ° C (optional)-W/O battery pack > 50 ° C
	Storage: -40°C to 70°C
Humidity	According to IEC 68-2-30/MIL-STD-810F, Method 507.45% to 95% RH, non-condensing
Altitude	According to IEC 68-2-13/MIL-STD-810F, Method 500.4
	Operating: 15,000 ft, non-operating: 40,000 ft
	Altitude change rate: 2,000 ft/min
Shock	According to IEC 68-2-27/MIL-STD-810F, Method 516.5
	Operating: 15 g, 11 ms, half sine wave
	Non-operating: 50 g, 11 ms, half sine wave
Vibration	According to IEC 68-2-6 / MIL-STD-810F, Method 514.5
	Operating: 10~57.5 Hz/0.075 mm, 57.5~500 Hz/1.0 g
	MIL-STD-810F, 514.5C1-high way truck vibration exposure
	Non-operating: 10~57.5 Hz/0.15 mm, 57.5~500 Hz/2.0 g
	MIL-STD-810F-514.5C-17 general minimum integrity exposure

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Drop	According to IEC 68-2-32 / MIL-STD-810F, Method 516.5
	- 3-foot-high free drop on steel plate, 4-foot-high free drop on plywood plate
	- 26 times/one machine (Panel close/Power off)
ESD	According to IEC1000-4-2
	Air Discharge: 0 KV~8 KV (included), no any error 8 KV~15 KV, allow soft error
	Contact data pin discharge: 0 KV~6 KV (included), no any error 6 KV~ 8 KV, allow soft error
Salt Fog *	5% Sodium Chloride (NaCl) during the entire exposure period measure the salt fog fallout rate and PH of the fallout solution at least at 48-hour intervals. Ensure the fallout is between 1 and 3 ml/80 cm^2/hr
Regulation	FCC part 15, Subpart B, C, Class B, UL, CUL, TUV, CE! , CB, CCC, WHQL, BSMI, E-Mark
Options	Removable Options:
	Easy changeable wireless modem in X-BAY: EDGE, EVDO, GPS ODD devices (Combo drive, DVD dual) Vehicle docking board (Backward compatible with M220)
	Factory Options:
	HDD heater Full travel membrane keyboard with backlight Rubber keyboard with backlight Blue tooth (class1) - TECOM Class I module BT3014 with Broadcom firmware v1.2

1.2 System Architecture

1.2.1 Function Description

1.2.1.1 CPU

➢ **Intel Mobile Yonah processor**

- First dual core processor for mobile (Yonah and Yonah low voltage skus)
- 667 MT/s (667 MHz) FSB support
- On-die, primary 32-KB instruction cache and 32-KB write back data cache
- On-die, 2 MB L2 cache with advanced transfer cache architecture
- Streaming SIMD Extension 2 (SSE2) and Streaming SIMD Extension 3 (SSE3)
- Support Intel architecture with dynamic execution
- Advanced gunning transceiver logic (AGTL+) bus driver technology
- Enhanced Intel SpeedStep technology to anable real-time dynamic switching between multiple voltage and frequency points
- Data prefetch logic
- 479-ball Micro-FCBGA package

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1.2.1.2 North Bridge & 3D Graphics DDR2 Chipset – Intel 945GM

➢ FSB Support

- AGTL+bus driver technology with integrated GTL termination resister (gated AGTL+receivers for reduced power)
- Supports 32-bit AGTL+host bus addressing
- 667 MT/s (667 MHz) and 533 MT/s (533 MHz) FSB support
- 2X address, 4X data
- Host bus dynamic bus inversion HDINV support
- 12 deep, in-order queue

➢ Integrated System Memory DRAM Controller

- Supports up to two DDR2 SDRAM channels (64 bit wide per channel)
- One SO-DIMM connecter per channel
- Maximum of two, double-sided unbuffered SO-DIMMs (4 rows populated)
- Minimum amount of memory supported is 128 MB (16 MB x 16-b x 4 devices x 1 row=128 MB), using 256 MB technology Serial ATA controller
- 256 MB, 512 MB and 1 GB technology using X8 and X16 devices
- Three memory channel organization are supported for DDR2

- Single channel
- Dual channel symmetric
- Dual channel asymmetric

- Support DDR2 400/533/667 devices
- Supports On-Die Termination (ODT) for DDR2
- Supports fast chip select mode
- Supports partial writes to memory using Data Mask signals (DM)
- Supports high-density memory package for DDR2 type devices
- Supports Reduced Power DDR2 (RPDDR2)
- Supports Intel Rapid Memory Power Management

➢ **External Graphics Using PCI Express Architecture Interface**

- One X16 (16 lanes) PCI Express port intended for graphics attach; fully compliant to the PCI Express base specification revision 1.0a
- Maximum theoretical realized bandwidth on interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when X16
- Automatic discovery, negotiation and training of link out of set
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI-X ordering)

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- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e. normal PCI 2.3 configuration space as a PCI-to-PCI bridge)
- Supports lane reversal and bit swapping

➢ Internal Graphics Controller

- Graphics core frequency

  - 2D Display core frequency at 133, 200 or 250 MHz @ Vcc=1.05 V depending on the host/ memory configurations

  - 3D Render core frequency at 133, 166, 250 MHz @Vcc=1.05 V depending on the host/ memory configurations

  - Intel® Smart 2D Display Technology

  - Intel® dual-frequency graphics technology support

  - Dynamic Video Memory Technology (DVMT) 3.0 support

- 3D graphics engine

  - DirectX* 9.0 support

  - OpenGL* 1.5 and 2.0 support

  - Zone rendering 2.0 support

- Analog CRT DAC interface support

  - Supports max DAC frequency up to 400 MHz

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  - 24-bit RAMDAC support
  - DDC2B compliant
  - Up to 2048x1536 resolution support

- Analog TV-out interface support
  - Integrated TV-out device supported on display pipes A and B
  - NTSC/PAL encoder standard formats supports
  - 480i/480p/576i/576p/720p/1080i/1080p modes supported
  - Tri-level Sync signal
  - Multiplexed output interface
  - Composite video with S-Video
  - S-Video
  - Component video
  - Up to 1024x768 resolution supported for NTSC/PAL
  - Macrovision, overscan scaling and flicker filtering support

- Serial Digital Video out Port (SDVO) interface support
  - Two SDVO ports are muxed with a subset of the external graphics interface using PCI Express architecture signals
  - Each SDVO port support display pixel rates up to 200 MP/s (600 MB/s)

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- Supports a variety display devices such as DVI, TV-out, LVDS .etc
- Supports hot plug and display
- Support for HDCP SDVO devices
- Support for Macrovision on SDVO TV-out devices
- Support for lane reversal

- Digital LVDS interface support
  - Integrated dual channel LVDS interface supported on display pipe B only
  - Compliant with ANSI/TIA/EIA-644-2001 spec
  - Supports 25 MHz to 112 MHz single/dual channel LVDS LCD interface with support for format of 1x18 bpp for TFT panels with single channel LVDS, 2x18 bpp for TFT panels with dual channels LVDS
  - Panel fitting, panning and center mode supported
  - Spread Spectrum Clocking (SSC) supported
  - Panel power sequencing compliant with SPWG timing specification
  - Integrated PWM or dedicated GMBus interface for LCD backlight inverter control
  - Intel® Display Power Savings Technology 2.0 support
  - Maximum UXGA panel size supported
  - Maximum WUXGA wide panel size supported

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- PCI Express x1 port support

  - One general purpose PCI Express port support

  - External graphics using PCI Express architecture and SDVO are functional in this mode

- Direct Media Interface (DMI)

  - Chip-to-chip interconnect between the GMCH and Intel 82801GBM

  - DMI X2 and DMI X4 configurations support

  - Bit swapping is supported

  - Lane reversal is supported

- Packing/power

  - 1466-ball micro-FCBGA (37.5 mm x 37.5 mm) with a 42-mil x 34-mil ball pitch

  - VCC (1.05 core supply)

  - VCCSM (DDR2=1.8 V I/O supply)

  - VCCHV (3.3 V high voltage supply)
    VCCA_CRTDAC (2.5 V CRT analog supply)
    VCC_SYNC (2.5 V HSYNC/VSYNC supply)

  - VCCD LVDS (1.5 V digital supply)
    VCCTX_LVDS (2.5 V Data/CLK Tx power supply)
    VCCA_LVDS (2.5 V LVDS analog supply)

- VCCA_TVBG (3.3 V TV DAC bnad gap supply)
  VCCD_TVDAC (1.5 V TV DAC supply)
  VCCDQ_TVDAC (1.5 V TV DAC quiet supply)
  VCCA_TVDACA (3.3 V TV-out Channel A supply)
  VCCA_TVDACB (3.3 V TV-out Channel B supply)
  VCCA_TVDACC (3.3 V TV-out Channel C supply)

- VCC3G (1.5 V PIC-E/DMI analog supply)
  VCC3A_GBG (2.5V PCI-E/DMI band gap supply)

- VCCA_HPLL (1.5 V host VCO supply)
  VCCA_MPLL (1.5 V system memory VCO)
  VCCD_HMPLL (1.5 V digital dividers supply)
  VCCA_3GPLL (1.5 V PCI-E PLL supply)
  VCCA_DPLLA/B (1.5 V Display A/B PLL supply)

1.2.1.3 System Frequency Synthesizer – ICS9LPR310

- ICS9LPR310 is a low power CK410M-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. ICS9LPR310 is driven with a 14.318 MHz crystal 667 MT/s (667 MHz) FSB support
- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318 MHz crystal, external crystal load caps are required for frequency tuning
- PEREQ# pins to support PCIEX power management
- Programmable watchdog safe frequency
- Low power differential clock outputs (No 50 ohm resistor to GND needed)

1.2.1.4 PCMCIA Controller – TI PCI 1520+TPS2224A

➢ **TI PCI 1520 – Card Bus Controller**

- The PCI1520, a dual-slot Card Bus controller designed to meet the PCI Bus power management interface specification for PCI to Card Bus bridges, is an ultra-low power high-performance PCI-to-Card Bus controller that supports two independent card sockets compliant with the PC card standard
- The PCI1520 provides features that make it the best choice for bridging between PCI and PC cards in both

notebook and desktop computers. The 1997 PC card standard retains the 16-bit PC card specification defined in PCI local bus specification and defines the new 32-bit PC card, Card Bus, capable of full 32-bit data transfers at 33 MHz. The PCI1520 supports any combination of 16-bit and Card Bus PC cards in the two sockets, powered at 5 V or 3.3 V, as required

- The PCI1520 is compliant with the PCI local bus specification and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during Card Bus PC card bridging transactions. The PCI1520 is also compliant with PCI bus power management interface specification

- Key Features

- 209-terminal MicroStar BGA ball-grid array (GHK/ZHK) package

- 2.5 V core logic and 3.3 V I/O with universal PCI interfaces compatible with 3.3 V 5 V PCI signaling environments

- Integrated low-dropout voltage regulator (LDO-VR) eliminates the need for an external 2.5 V power supply

- Mix-and-match 5 V/3.3 V 16-bit PC cards and 3.3 V Card Bus cards

- Two PC card or Card Bus slots with hot insertion and removal

- Serial interface to TI TPS222X dual-slot PC card power switch

- Burst transfers to maximize data throughput with Card Bus cards

- Interrupt configurations: parallel PCI, serialized PCI, parallel ISA and serialized ISA

- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID

- Pipelined architecture greater than 130 Mbps throughout from Card Bus-to-PCI and from PCI-to-Card Bus

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➢ TPS2224A – PCMCIA and Card Bus Power Switch

- The TPS2224A Card Bus power-interface switch provide an integrated power management solution for two PC card sockets. These devices allow the controlled distribution of 3.3 V, 5 V, 12 V to each card slot. The current-limiting and thermal protection features eliminate the need for fuses. Current-limiting reporting helps the user isolate a system fault. The switch Rds (on) and current-limiting values have been set for the peak and average current requirements stated in the PC card specification

- key features

  - Fast current limit response time
  - Fully integrated VCC and VPP switching for 3.3 V, 5 V and 12 V
  - Meets current PC card standards
  - VPP output selection independent of VCC
  - 12 V and 5 V supplies can be disabled
  - TTL-Logic compatible inputs
  - Short-circuit and thermal protection
  - 140 µA (Typical) quiescent current from 3.3 V input
  - Break-before-make switching
  - Power-on reset
  - 40 °C to 85 °C operating ambient temperature range
  - 32-pin SSOP package

1.2.1.5 Read Only Memory (Flash ROM)

- FWH bus interface
- Single 3.3 V operations
- 3.3 V – volt Read
- 3.3 V – volt Erase
- 3.3 V – program
- Fast program operation
- VPP=12 V
- Byte-by-Byte programming: 9 µs (typ.)
- Fast erase operation
- Fast read access time: Tkg 11 ns
- Endurance: 30 K cycles (typ.)
- Twenty-year data retention
- 16 even sectors with 64 K bytes
- Any individual sector can be erased
- Hardware protection
- #TBL supports 64-Kbyte Boot Block hardware protection

- #WP supports the whole chip except boot block hardware protection
- Hardware features
- Latched address and data
- TTL compatible I/O
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
- Toggle bit
- Data polling
- Low power consumption
- Read active current:15 mA (typ. for FWH mode)
- VPP input pin
- Acceleration (ACC) function accelerates program timing
- Hardware reset pin (#RESET)
- Reset the internal state machine to the read mode
- Ready/#Busy output (RY/#BY)
- Detect program or erase cycle completion
- Dual BIOS function
- Full-chip partition with 8 M-bit or dual-block partition with 4 M-bit

- Available packages: 32L PLCC, 32L STSOP, 40L TSOP (10x20 mm), 32 PLCC lead free, 32L STSOP lead free and 40L TSOP (10x20 mm) lead free

1.2.1.6 Keyboard Controller

The H8S/2140 is a high-speed central processing unit with an internal 32-bit architecture that is upward-compatible with the H8/300 and H8/300H CPUs. The H8S/2000 CPU has sixteen 16-bit general registers, can address a 16-Mbyte linear address space and is ideal for real-time control.

Detail specification as below:

- ➢ Bus Controller
  - Basic bus interface
  - Burst ROM interface
  - Idle cycle insertion
  - Bus arbitration function
- ➢ Data Transfer Controller
  - Transfer is possible over any number of channels
  - Three transfer modes
  - One activation source can trigger a number of data transfers (chain transfer)
  - Direct specification of 16-Mbyte address space is possible

- Activation by software is possible
- Transfer can be set in byte or word units
- A CPU interrupt can be requested for the interrupt that activated the DTC
- Module stop mode can be set

➢ 16-Bit Free-Running Timer (FRT)

- Selection of four clock sources
- Two independent comparators
- Four independent input capture channels
- Counter clearing
- Seven independent interrupts
- Special functions provided by automatic addition function

➢ 8-Bit PWM Timer (PWM)

- Operable at a maximum carrier frequency of 625 KHz using pulse division (at 10 MHz operation)
- Duty cycles from 0 to 100% with 1/256 resolution (100% duty realized by port output)
- Direct or inverted PWM output and PWM output enable/disable control

- 14-Bit PWM Timer (PWMX)
  - Division of pulse into multiple base cycles to reduce ripple
  - Two resolution settings
  - Two base cycle settings
  - Four operating speeds
  - Four operation clocks (by combination of two resolution settings and two base cycle settings)

- 8-Bit Timer (TMR)
  - Selection of clock sources
  - Selection of three ways to clear the counters
  - Timer output controlled by two compare-match signals
  - Cascading of TMR_0 and TMR_1
  - Multiple interrupt sources for each channel

- Timer Connection
  - Five input pins and four output pins, all of which can be designated for phase inversion
  - An edge-detection circuit is connected to the input pins, simplifying signal input detection
  - TMR_X can be used for PWM input signal decoding

- TMR_X can be used for clamp waveform generation

➢ Watchdog Timer (WDT)

- Selectable from eight (WDT_0) or 16 (WDT_1) counter input clocks
- Switchable between watchdog timer mode and interval timer mode

➢ Serial Communication Interface (SCI & IrDA)

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability
- The on-chip baud rate generator allows any bit rate to be selected
- Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

➢ Bus Interface (IIC)

- Selection of addressing format or non-addressing format
- Conforms to Philips I2Cbus interface (I2Cbus format)
- Two ways of setting slave address (I2Cbus format)
- Start and stop conditions generated automatically in master mode (I2C bus format)
- Selection of the acknowledge output level in reception (I2C bus format)

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- Automatic loading of an acknowledge bit in transmission (I2C bus format)
- Wait function in master mode (I2C bus format)
- Wait function (I2C bus format)
- Interrupt sources
- Selection of 16 internal clocks (in master mode)
- Direct bus drive (SCL/SDA pin)
- Automatic switching from formatless mode to I2C bus format (IIC_0 only)

➢ Host Interface X-Bus Interface

- Control of the fast GATE A20 function
- Shutdown of the XBS module by the HIFSD pin
- Five host interrupt requests

➢ Keyboard Buffer Controller

- Conforms to PS/2 interface specifications
- Direct bus drive (via the KCLK and KD pins)
- Interrupt sources: on completion of data reception and on detection of clock edge
- Error detection: parity error and stop bit monitoring

➢ Host Interface LPC Interface (LPC)

- Supports LPC interface I/O read cycles and I/O write cycles
- Has three register sets comprising data and status registers
- Supports SERIRQ
- Eleven interrupt sources

➢ A/D Converter

- 10-bit resolution
- Input channels: eight analog input channels and 16 digital input channels
- Analog conversion voltage range can be specified using the reference power supply voltage pin (AVref) as an analog reference voltage
- Conversion time: 13.4 µs per channel (at 10-MHz operation)
- Two kinds of operating modes
- Four data registers
- Sample and hold function
- Three kinds of conversion start
- Interrupt request

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- D/A Converter
  - 8-bit resolution
  - Two output channels
  - Conversion time: Max. 10 µs (when load capacitance is 20 pF)
  - Output voltage: 0 V to AVref
  - D/A output retaining function in software standby mode
- I/O ports
  - Ten I/O ports (ports 1 to 6, 8, 9, A, and B), and one input-only port (port 7)
- Interrupt Controller
  - Two interrupt control modes
  - Priorities settable with ICR
  - Independent vector addresses
  - Thirty-one external interrupts
  - DTC control

➢ Power-Down Modes

- Medium-speed mode
- Subactive mode
- Sleep mode
- Subsleep mode
- Watch mode
- Software standby mode
- Hardware standby mode
- Module stop mode

1.2.1.7 Super I/O – SMSC SIO10N268

- ➢ 3.3 Volt Operation (5 Volt Tolerant)
- ➢ PC99, PC01, ACPI 1.0 Compliant
- ➢ LPC Interface Design
- ➢ X-Bus Interface (LPC Mode Only)
  - Three chip selects (Two I/O and one memory)
  - 8-Bit data transfers
  - Support for up to 2 MB flash
  - Interfaces with 3 V memory devices
  - Support for up to two external I/O components
  - Offers three modes of operation for I/O devices
  - Provides FWH emulation
- ➢ Serial IRQ Compatible with Serialized IRQ Support for PCI Systems
- ➢ Programmable Wake-up Event (PME) Interface
- ➢ 33 General Purpose Input/Output Pins
- ➢ System Management Interrupt

M230 N/B Maintenance

- 2.88 MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B floppy disk controller
  - Software and register compatible with SMSC's proprietary 82077AA compatible core
  - Supports two floppy drives directly
  - Configurable open drain/push-pull output drivers
  - Supports vertical recording format
  - 16-byte data FIFO
  - 100% IBM compatibility
  - Detects All overrun and under run conditions
  - Sophisticated Power Control Circuitry (PCC) including multiple Power Down Modes for reduced power consumption
  - DMA enable logic
  - Data rate and drive control registers
  - 480 addresses, up to 15 IRQ and four DMA options

- Floppy Disk Available on Parallel Port Pins (ACPI Compliant)
  - Enhanced digital data separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps data rates

- Programmable precompensation

➢ Serial Ports

- Four full function serial ports
- High speed NS16C550 compatible UARTs with Send/Receive 16-byte FIFOs
- Supports 230 K and 460 K baud
- Programmable baud rate generator
- Modem control circuitry
- 480 address and 15 IRQ options

1.2.1.8 1394B Controller – TI TSB82AA2

- Single 3.3 V supply (1.8 V internal core voltage with regulator)
- 3.3 V and 5 V PCI signaling environments
- Serial bus data rates of 100M bits/s, 200M bits/s, 400M bits/s and 800M bits/s
- Physical write posting of up to three outstanding transactions
- Serial ROM or boot ROM interface supports 2-wire serial EEPROM devices
- 33 MHz/64 bit and 33 MHz/32 bit selectable PCI interface
- PCI burst transfers and deep FIFOs to tolerate large host latency
- Transmit FIFO – 5 K asynchronous
- Transmit FIFO – 2 K isochronous
- Receive FIFO – 2 K asynchronous
- Receive FIFO – 2 K isochronous
- D0, D1, D2, and D3 power states and PME events per the PCI Bus power management interface specification
- Programmable asynchronous transmit threshold
- Isochronous receive dual-buffer mode
- Out-of-order pipelining for asynchronous transmit requests
- Register access fail interrupt when the PHY SYSCLK is not active

M230 N/B Maintenance

- Initial bandwidth available and initial channels available registers
- Digital video and audio performance enhancements
- Fabricated in advanced low-power CMOS process
- Multifunction terminal (MFUNC terminal 1)
- PCI_CLKRUN protocol per the PCI Mobile Design Guide
- General-purpose I/O
- CYCLEIN/CYCLEOUT for external cycle timer control for customized synchronization
- Packaged in 144-terminal LQFP (PGE)

1.2.1.9 Audio Codec – Realtek ALC260

- Single-chip multi-bit Sigma-Delta converters with high S/N ratio
- 1 stereo DAC supports 16/20/24-bit PCM format with 44.1/48/96/192 KHz sample rate
- 2 stereo ADCs support 16/20-bit PCM format with 44.1/48/96 KHz sample rate
- Applicable for 2-Channel 192 KHz DVD-Audio solutions
- LINE-OUT, HP-OUT, LINE1, LINE2, MIC1 and MIC2 are stereo input and output re-tasking
- MONO line level output to subwoofer speaker for 2.1 channel applications
- High-quality differential CD analog input
- External PCBEEP input is applicable, and internal BEEP generator is integrated
- Power-Off CD mode supported
- Power management and enhanced power saving features
- Power support: Digital: 3.3 V; Analog: 3.3 V/5.0 V
- Selectable 2.5 V/3.75 V VREFOUT
- Two jack detection pins (each designed to detect 4 jacks)
- Supports 44.1 K/48 K/96 kHz/192 kHz S/PDIF output
- Supports 44.1 K/48 K/96 KHz S/PDIF input
- 48-pin LQFP packages (lead (Pb)-free package also available)

M230 N/B Maintenance

- Supports external volume knob control
- Reserve analog mixer architecture is backwards compatible with AC'97
- –64 dB ~ +30 dB with 1 dB mixer gain for fine volume control
- Impedance sensing capability for each re-tasking jack
- Built-in headphone amplifier for each re-tasking jack
- Supports GPIOs (General purpose input/output) for customized applications
- Hardware copyright protection for DVD-Audio
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- A3D™ compatible
- I3DL2 compatible
- HRTF 3D positional audio
- Emulation of 26 sound environments to enhance gaming experience
- 10-band software equalizer
- Voice cancellation and key shifting in Karaoke mode
- Enhanced configuration panel and device sensing wizard to improve user experience
- Content copy protection for S/PDIF interface

- Power management setting
- Microphone Acoustic Echo Cancellation (AEC) and Beam Forming (BF) technology for voice application
- Mono/Stereo Microphone noise suppression

1.2.1.10 LAN – Broadcom BCM5752

- Integrates TPM 1.2 security functionality enabling OEMs to offer this high level of PC security as a standard feature
- Enables TPM-ready security platforms for next Microsoft OS (Longhorn)
- Integrates 10/100/1000 BASE-T transceiver and media access controller

MiTac Secret Confidential Document

1.2.1.11 Mobility VGA Chipset – ATI M54CSP128

The M54/M52 provides the fastest and most advanced 2D, 3D and multimedia graphics performance for notebooks. The M54/M52 supports Shader Model 3.0, advanced memory interface technology, a brand new display controller and a consumer electronics (CE) quality TV (NTSC/PAL) encoder.

The M54 is based on PCI Express technology and leverages a brand new graphics architecture. Based on 90 nm micron process technology, the M54 will deliver a 16-lane PCI Express bus interface and lead-free ASIC

Features in Detail:

➢ 2D Acceleration Features

- A highly optimized 128 bit engine, capable of processing multiple pixels/clock
- Hardware acceleration is provided for Bitblt, line drawing, polygon and rectangle fills, bit masking, monochrome expansion, panning and scrolling, scissoring, and full ROP support (including ROP3)
- Optimized handling of fonts and text using ATI proprietary techniques
- Game acceleration including support for Microsoft's DirectDraw: Double Buffering, Virtual Sprites, Transparent Blit, and Masked Blit
- Acceleration in 8/15/16/32 bpp modes
- Support for WIN 2000 & WIN XP GDI extensions: Alpha BLT, Transparent BLT, Gradient Fill
- Hardware cursor support up to 64x64x32 bpp, with alpha channel for direct support of WIN 2000 & WIN XP alpha cursor standard

➢ 3D Acceleration Features

- DirectX9 Shader Model 3.0 support
- Full DX9 conformance, including floating point per component at full speed
- Support for 2X AA, 4X AA and 6X AA subsamples, with little performance loss in most cases
- Advanced AA quality algorithms, generating visuals that are superior to other solutions with an equivalent number of samples
- 2X/4X/8X/16X anisotropic filtering modes. Adaptive algorithm with bi-linear (performance) and tri-linear (quality) options

M230 N/B Maintenance

- Dedicated geometry acceleration for Direct3D and OpenGL, which incorporates 2 parallel Vector/Scalar Engines performing HW transformation, clipping and lighting
- 2 full vertex processors in the VAP (Vertex Assembler & Processor)

➢ Motion Video Acceleration Features

- Video scaling and fully programmable YCrCb to RGB color space conversion for full-screen/full-speed video playback and fully adjustable color controls
- Hardware I2C
- VIP 2.0 with multi channel DMA transfer
- Front end scaler support for 8, 15, 16, and 32 bpp color depths
- Back end overlay/scaler supports up to 8x4 tap filtering, and always ensures at least 4x2 tap filtering even in extreme cases. 4x4 tap is typical. Back-end scaler also supports upscaling and downscaling, filtered scaling of all supported YUV formats, RGB32 and RGB15/16, and filtered display of images up to 1536 pixels wide
- MPEG-4 simple profile suppor
- Adaptive de-interlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, by analyzing image and using optimal de-interlacing function on a per-pixel basis

➢ Dual Display Features

- Improved 64-bit display controller with symmetric display capabilities
- Two triple 10-bit palette DACs (DAC and DAC2) with gamma correction for true WYSIWYG color. Pixel

rates up to 400 MHz standard

- Dual RGB CRT output
- One C Y COMP output plus second RGB CRT output from second DAC
- Dual displays (LCD/DVI, DVI/CRT, LCD/TV, CRT/TV, etc.), with completely independent resolution, refresh rates, h/w icon & h/w cursor and display data
- Hardware cursor up to 64x64 pixels in 2 bpp, full color AND/XOR mix and full color 8-bit alpha blend
- Primary display supports VGA and accelerated modes, video overlay and hardware cursor
- Secondary display supports TV-out or CRT. It supports accelerated modes, video overlay, and hardware cursor; however, it does not support VGA. Modes supported include 800x600 and 16:9 modes such as 848x480, with user flexibility for moving and sizing the screen MPEG-4 simple profile support
- Support for up to 4 K x 4 K resolution display

➢ Digital Display Support

- Support for fixed resolution displays (e.g. panels) from VGA (640x480) to wide UXGA (1920x1200) resolution with full ratiometric expansion ability for source modes up to 1400 x 1050 with standard display timing, or up to 1920x1440 with reduced blanking timing. Higher resolution panels and digital CRTs may be possibly supported-contact ATI for details
- Improved auto expansion
- Optional auto-centering mode to display desktop at native size without ratiometric expansion
- Support for VGA text modes in centering panel modes (up to approximately 165 MHz pixel frequency)

MiTac Secret Confidential Document

- Support for reduced blanking intervals, as defined by VESA

➢ Bus Support Features

- PCI Express 1.0a and PCI Express 1.1 compliant. PCI Express is the latest generation I/O interconnect architecture which replaces conventional PCI and AGP buses in new PC platforms. Refer to PCI-SIG for specifications relating to PCI Express architecture
- Native X16 PCI Express bus interface
- Supports X1, X2, X4, X8, X12 and X16 lane widths
- Supports X16 lane reversal where the receiver on lanes 0 to 15 on the graphics endpoint are mapped to the transmitter on lanes 15 down to 0 on the root complex
- Supports X16 lane reversal where the transmitter on lanes 0 to 15 on the graphics endpoint are mapped the receiver on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex)
- Supports X1, X2, X4, X8, X12 and X16 polarity inversion
- Supports “Mobile Graphics Low-Power Addendum to the PCI Express Base Specification 1.0”

➢ Memory Support Features

- 256/128/64-bit memory interface using DDR1 or DDR2 SDRAM/SGRAM or GDDR3 SDRAM (except M52-T) to build 16/32/64/128/256/512 MB configurations
- Support for SSTL-1.8 memory interface

M230 N/B Maintenance

➢ Power Management Features

- Single chip solution in 90 nm micron CMOS technology
- Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management
- Static and Adynamic Power Management support (APM as well as ACPI) with full VESA DPM and energy star compliance
- Full PowerPlayTM 6.0, including enhanced Power on Demand support
- The chip power management support logic supports four device power states - on, standby, suspend and off - defined for the OnNow architecture. Each power state can be achieved by software control bits
- Clocks to every major functional block are controlled by a unique dynamic clock switching technique which is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation

➢ Internal LVDS Spread Spectrum Support

- The M54/M52 spread spectrum controller is capable of generating a triangular frequency modulation profile. The amount of spread and the modulation frequency is fully programmable
- Only the LVDS display is available to be spread (i.e., 1 PLL)

➢ External Spread Spectrum Support

- Memory and/or core clock spread spectrum support via the GPIO16 pin
- External spread spectrum supported for TMDS or LVDS transmitters via the GENERICC/GENERICD pin

M230 N/B Maintenance

➢ PC Design Guide Compliance

- Fully compliant with Windows Logo program requirements for all target Operating Systems. This includes both the current Logo requirements and the future (draft) requirements that will be enforced during the lifespan of the product
- Fully compliant with Mobile PCI rev 1.0
- Bi-endian support for compliance on a variety of processor platforms

➢ Test Capability Features

- Full scan implementation on the digital core logic which provides high fault coverage through ATPG (Automatic test pattern generation vectors)
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules
- A JTAG test mode (which is largely compliant with the IEEE 1149.1 standard) including internal scan chain for access to chip-level test functions and for board level connectivity testing
- Integrated hardware diagnostic tests performed automatically upon initialization
- High quality components through built-in scan and chip diagnostics
- Improved access to the analog modules and PLLs in the M54/M52 in order to allow full evaluation and characterization of these modules

➢ Other Features

- Support for serial ROM video BIOS
- Support for 32 and 64-bit operating systems based on Intel, AMD and PowerPC CPUs
- HW cursor support for monochrome, color and alpha blended cursors
- GDI support for Alpha & Transparent BLTs, as well as Gradient Fills

➢ Compliance with Wassenaar Agreement

- 3D vector rate (as defined by the Wassenaar Agreement) is 58-78 M 10-pixel vectors/sec

1.2.1.12 USB Bluetooth (option) – TECOM BT3014

- Bluetooth Specification V.1.2 compliant
- Bluetooth spec 1.1 compatible
- Bluetooth protocol stacks and profiles support is optional
- Indoor coverage range up to 50 m typically in general environments for the Class 1 output power with 0dBi omni-directional antenna
- Outdoor coverage range up to 100 m typically in open site for the Class 1 output power with 0dBi omni-directional antenna
- Output power controllable
- Max data rate 720 kbps

1.2.1.13 Fax/Modem – Askey 1456VQL-T1 (INT-LF)

- HD audio, AC’97, MC’97 2.2 compliant
- V.44, V.42, V.42bis and MNP ™ Class 5 data compression
- Low-power standby mode
- 3.3 V to 5 V power supply
- Compliant with FCC, CTR21, JATE and other PTTs
- Auto sensing host interface to select AC’97 or HD audio
- OperationtTemperature/humidity: 0 °C/0%~60 °C/90%
- Storage temperature/humidity: -20 °C/0%~70 °C/90%

1.2.1.14 South Bridge ICH7-M

➢ PCI Bus Interface

- Supports PCI Revision 2.3 Specification at 33 MHz
- Supports up to 6 master devices on PCI
- NEW: Six available PCI REQ/GNT pairs
- Support for 64-bit addressing on PCI using DAC protocol

M230 N/B Maintenance

- PCI Express Interface
  - 4 PCI Express root ports
  - NEW: 2 Additional PCI Express root ports (Not available on all ICH7 SKUs)
  - Supports PCI Express 1.0a
  - Ports 1-4 can be statically configured as 4x1,or 1x4
  - Support for full 2.5 Gb/s bandwidth in each direction per x1 lane
  - Module based Hot-Plug supported (e.g., Express Card)
- Integrated Serial ATA Host Controller
  - two ports (Mobile Only)
  - Integrated AHCI controller (Not available on all ICH7 SKUs)
- Integrated IDE Controller
  - Independent timing of up to two drives
  - Ultra ATA 100/66/33, BMIDE and PIO modes
  - Tri-state modes to enable swap bay
- USB2.0

- Includes four UHCI host controllers that support eight external ports
- Includes one EHCI high-speed USB 2.0 host controller that supports all eight ports
- Includes one USB 2.0 High-speed debug port
- Supports wake-up from sleeping states S1-M–S5
- Supports legacy keyboard/mouse software

➢ Intel® High Definition Audio Interface

- PCI Express endpoint
- Independent Bus Master logic for eight general purpose streams: four input and four output
- Support three external Codecs
- Supports variable length stream slots
- Supports multichannel,, 32-bit sample depth, 92 KHz sample rate output
- Provides mic array support
- Allows for non-48 KHz sampling output
- Support for ACPI device states
- NEW: Docking support
- NEW: Low voltage mode

- Interrupt Controller
  - Support up to eight PCI interrupt pins
  - Supports PCI 2.3 message signaled interrupts
  - Two cascaded 82C59 with 15 interrupts
  - Integrated I/O APIC capability with 24 interrupts
  - Supports processor system bus interrupt delivery

- 1.05 V operation with 1.5 V and 3.3 V I/O
  - 5V tolerant buffers on IDE, PCI, USB over-current and legacy signals

- Timers Based on 82C54
  - System timer, refresh request, speaker tone output

- Power Management Logic
  - ACPI 2.0 compliant
  - ACPI-defined power states (C1–C4, S1-M, S3–S5)
  - ACPI power management timer
  - Support for “Intel® SpeedStep^{TM} technology” processor power control
  - Support for “Deeper Sleep” power state

M230 N/B Maintenance

- PCI CLKRUN# and PME# support
- SMI# generation
- All registers readable/restorable for proper resume from 0 V suspend states
- Support for APM-based legacy power management for non-ACPI Desktop and Mobile implementation

- ➢ External Glue Integration
  - Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
  - Integrated Pull-down and Series resistors on USB
- ➢ NEW: Serial Peripheral Interface(SPI) for Serial and Shared Flash
- ➢ Firmware Hub (FWH) Interface supports BIOS memory size up to 8 MB
- ➢ Low Pin Count (LPC) Interface
  - Supports two Master/DMA devices
  - Support for Security Device(Trusted Platform Module) connected to LPC
- ➢ Enhanced DMA Controller
  - Two cascaded 8237 DMA controllers
  - Supports LPC DMA

M230 N/B Maintenance

- Real-Time Clock

  - 256-byte battery-backed CMOS RAM
  - Integrated oscillator components
  - Lower Power DC/DC Converter implementation

- System TCO Reduction Circuits

  - Timers to generate SMI# and Reset upon detection of system hang
  - Timers to detect improper processor reset
  - Integrated processor frequency strap logic
  - Supports ability to disable external devices

- SMBus

  - Flexible SMBus/SMLink architecture to optimize for ASF
  - Provides independent manageability bus through SM-Link interface
  - Supports SMBus 2.0 Specification
  - Host interface allows processor to communicate via SMBus
  - Slave interface allows an internal or external microcontroller to access system resources
  - Compatible with most two-wire components that are also I2C compatible

- NEW: 1.05 V Core Voltage
- Integrated 1.05 V Voltage Regulator (INTVR) for the Suspend and LAN wells
- GPIO: TTL, open-drain, inversion
- Package 31x31 mm 652 mBGA

1.2.1.15 LED Indicators

There are 13 LED indicators locate on the system housing, the detail shows on the follows table:

LED Number	**Functions**	**LED color**	**Remark**
LED BD HD1	Power on/Suspend	Green/Red	Power on: Green LED on, Suspend: Red LED on.
LED BD HD2	HDD	Amber	If HDD in accessing, LED on
LED BD HD4	Num Lock	Green	Keyboard Number Lock
LED BD HD5	Caps Lock	Green	Keyboard Caps Lock
LED BD HD3	Scroll Lock	Green	Keyboard Scroll Lock
M/BD D34	CDROM	Amber	If ODD in accessing, LED on
M/BD D33	Battery Low	Amber	If battery in Low state, amber LED blinks.
M/BD D32	Battery Charge Status	Amber /Green	If AC exist, amber LED on when battery in charging, Green LED on if battery full.
M/BD D35	Wireless LAN	Green	When wireless LAN link, Green LED on.
M/BD D36	XBAY GPRS module	Amber /Green	If GPRS module exist, green LED on, and amber LED on if the module active.
M/DB D37	LAN	Amber /Green	If the Ethernet LAN link, amber LED on, and green LED on if the Ethernet LAN active.
M/BD D836	Touch Pad ON/Off	green	If Touch Pad disable, LED on
M/BD D31	AC IN/HDD Low Temp.	Green/Red	If AC exists, Green LED on. If HDD temperature below 2°C or ambient temperature over 60°C, Red LED blinks.

1.2.1.16 Mini PCI-E Interface

- Mechanical dimension support the Mini Card
- Mini PCI_E Interface – Pin out of System Connector

Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	3.3VS
3	WLAN_AACTIVE	4	GROUND
5	BT_ACTIVE	6	1.5VS
7	PCIECLKREQ2#	8	NC
9	GROUND	10	NC
11	CLK_PCIE_S1#	12	NC
13	CLK_PCIE_S1	14	NC
15	GROUND	16	NC
17	TP	18	GROUND
19	TP	20	MINI_PD#
21	GROUND	22	BUF_PLT_RST#
23	PCIE_RXN3	24	3.3V
25	PCIE_RXP3	26	GROUND
27	GROUND	28	1.5VS
29	GROUND	30	SMBCLK
31	PCIE_TXN3	32	SMBDATA
33	PCIE_TXP3	34	GROUND
35	GROUND	36	NC
37	NC	38	NC
39	NC	40	GROUND
41	NC	42	S1_LED0
43	NC	44	S1_LED1
45	NC	46	S1_LED2
47	NC	48	1.5VS
49	NC	50	GROUND
51	NC	52	3.3V
53	GROUND	54	GROUND

1.2.1.17 Buttons

- Power on (I/O BD: HSW1) – Push button for power on and off control

1.2.1.18 I/O Ports

➢ RJ-11 Modem Line Connector

Pin	Signal Name	Power On default Direction	S0 State	S3 State	S4 State	Description
1	TIP	Active	Active	Active	Power off	Transmit Data Tip
2	RING	Active	Active	Active	Power off	Transmit Data Ring

➢ RJ-45 With LED Connector

Pin	Name	default	S0 State	S3 State	S4 State	Description
1	TX+	OD				Data Transmit and Receive
2	TX-	OD				Data Transmit and Receive
3	RX+	OD				Data Transmit and Receive
4	TRD2+	OD				Data Transmit and Receive
5	TRD2-	OD				Data Transmit and Receive
6	RX-	OD				Data Transmit and Receive
7	TRD3+	OD				Data Transmit and Receive
8	TRD3-	OD				Data Transmit and Receive

- Infrared Interface Supporting IRDA Format -HSDL 3602 (288003602002)
  - Fully compliant to IrDA 1.1 physical layer specifications (9.6 Kb/s to 4 Mb/s operation)
  - Typical link distance of =1.0 m
  - Low power operation of 3.3 V
  - Small module size of height 4.0 mm, width 12.2 mm, depth 5.1 mm
  - Complete shutdown (TXD, RXD, PIN Diode)
  - Low shutdown current of 10 nA typical
  - Single Rx data output allowing speed select by FIR select pin
  - Excellent noise immunity with integrated EMI Shield
  - Edge detection input feature preventing the LED from long turn-on time
  - Interface to various super I/O and controller devices
  - Designed to accommodate light loss with Cosmetic Window

Pin	Signal Name	Power On default Direction	S0 State	S3 State	S4 State	Description
1	VCC	Power off	+3V	Chip Power off	Power off	Supply Voltage
2	AGND	Ground	Ground	Ground	Ground	Analog Ground
3	FIR_SEL	In	Out	Chip Power off	Power off	FIR Select
4	MD0	In	Out	Chip Power off	Power off	Mode 0
5	MD1	In	Out	Chip Power off	Power off	Mode 1
6	NC					
7	GND	Ground	Ground	Ground	Ground	Ground
8	RXD	In	In	Chip Power off	Power off	Receiver Data
9	TXD	OUT	OUT	Chip Power off	Power off	Transmitter Data
10	LEDA	OUT	OUT	Chip Power off	Power off	LED Anode

- ➢ USB Ports-FOXCONN USB113C – K1 (MiTAC 331040004039)

Pin #	Signal	default	S0 State	S3 State	S4 State	Description
1	USB1_5V	0V	5V	5V	5V	Supply voltage
2	USB1-	Low	I/O	Low	Low	USB Differential Data Minus
3	USB1+	Low	I/O	Low	Low	USB Differential Data Plus
4	GND	Ground	Ground	Ground	Ground	Ground

- ➢ Antenna Switch Connector (MiTAC 297150100015)
  - It passes antenna signal from system to docking for using vehicle dock

- POGO Docking Port Connector – (MiTAC 796115000001)

Pin #	Signal name	default	S0 State	S3 State	S4 State	Description
1	VDOCK_POGO	In, 19V	In	In	In	Support mother board and battery charge
2	DVMAIN_POGO	OUT, 19V	OUT	OUT	OUT	Support docking board
3,4,6	Ground	Ground	Ground	Ground	Ground	Ground
5	P_H8_SM_DATA	Hi-Z	I/O	I/O	Hi-Z	SMBus Data
8	P_H8_SM_CLK	Hi-Z	I/O	I/O	Hi-Z	SMBus Clock
7	P_USB5+	Low	I/O	Low	Low	USB Differential Data Plus
10	P_USB5-	Low	I/O	Low	Low	USB Differential Data Minus
9	P_DOCK_RI#		I			Ring indicator
11	P_SPDIFOUT		O			SPIDFOUT Signal
12	P_USBOC#5		I			USB over current to USB HUB
13	P_USB4+	Low	I/O	Low	Low	USB Differential Data Plus
16	P_USB4-	Low	I/O	Low	Low	USB Differential Data Minus
14	P_SUSB#		O			S3 control
15	+3V_POGO	Out, 3.3V	Out, 3.3V	Out, 3.3V	Out, 3.3V	+3,3V POWER
17,18	+5V_POGO	Out, 5V	Out, 5V	Out, 5V	Out, 5V	+5V POWER
19	POGO_DOCK_IN		I			Dock sense
20	P_PWRON_CARKEY		I			Ignition input
21	+5VA_POGO	Out, 5V	Out, 5V	Out, 5V	Out, 5V	Supply voltage
22	AGND	Ground	Ground	Ground	Ground	Ground
23	P_MIC		I			Microphone Input Signal
24	P_AOUT_L		O			Line Out Left Signal
25	P_AOUT_R		O			Line Out Right Signal

- Serial Port Connector – (MiTAC 331040009005)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	COM1DCD#	IN				COM1 Carrier detector signal
2	COM1RXD	IN				COM1 Received data signal
3	COM1TXD	O				COM4 Transmitted data signal
4	COM1DTR#	O				COM1 Data terminal ready signal
5	Shield-ground	Ground				Ground
6	COM1DSR#	IN				COM1 Data set ready signal
7	COM1RTS#	O				COM1 Request to send signal
8	COM1CTS#	IN				COM1 Clear to send signal
9	COM1RI#	IN				COM1 Ring indicator signal

- Micphone Connector – (MiTAC 331040005015)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	GND					GND
2	Mic in					Microphone Input
3	NC					
4	NC					
5	NC					

M230 N/B Maintenance

- Parallel Port Connector – (MiTAC 331040009005)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	P_STB#	O				PIO Strobe
2	P_LPD0	I/O				PIO Data bit0 signal
3	P_LPD1	I/O				PIO Data bit1 signal
4	P_LPD2	I/O				PIO Data bit2 signal
5	P_LPD3	I/O				PIO Data bit3 signal
6	P_LPD4	I/O				PIO Data bit4 signal
7	P_LPD5	I/O				PIO Data bit5 signal
8	P_LPD6	I/O				PIO Data bit6 signal
9	P_LPD7	I/O				PIO Data bit7 signal
10	D/ACK#	I				PIO Printer Acknowledge
11	D/BUSY	I				PIO Printer Busy
12	D/PE	I				PIO Printer Paper End
13	D/SLCT	I				PIO Printer Selected Status
14	D/AFD#	O				PIO Auto Feed
15	D/ERR#	I				PIO Printer Error
16	D/INIT#	O				PIO Printer Initiate
17	D/SLIN#	I				PIO printer Select Input
18,19,20,21,22,23,24,25	Shield-ground	Ground				Ground

- VGA Port Connector – (Mitac 331040009005)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	CRT_RED					CRT RED SIGNAL
2	CRT_GREEN					CRT GREEN SIGNAL
3	CRT_BLUE					CRT BLUE SIGNAL
4	NC					No Connect
5	Ground					Ground
6	Ground					Ground
7	Ground					Ground
8	Ground					Ground
9	NC					No Connect
10	Ground					Ground
11	NC					No Connect
12	CRT_DDCDATA					CRT DDC Data Signal
13	CRT_HSYNC					CRT Horizontal Synchronization
14	CRT_VSYNC					CRT Vertical Synchronization
15	CRT_DDCCLK					CRT DDC Clock Signal

- 1394B Port Connector (MiTAC 291000000905)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	TPB0-	I/O				Differential signal
2	TPB0+	I/O				Differential signal
3	TPA0-	I/O				Differential signal
4	TPA0+	I/O				Differential signal
5	Shield-ground					Ground
6	Shield-ground					Ground
7	NC					No Connection
8	VCC					19V
9	Shield-ground					Ground

- Stereo Jack – (MiTAC 331840010019)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	DECT HP#/OPT					Audio and Optical Fiber Device detect
2	Line out left					Audio Line out left signal
3	Line out right					Audio Line out right signal
4	AGND					Audio ground
5	Device detect					Audio Device detect
6	NC					No Connection
7	SPDIFOUT					Optical Fiber
8	VCC					3V
9	GND					Ground
10	NC					No Connection

1.2.1.19 Internal Connector Definition

- LCD Connector (MiTAC 291000005017)-1

Pin #	Signal name	default	S0 State	S3 State	S4 State	Purpose
1	LCDVCC	O				3 V with fuse controlled by EN VDD video
2	LCDVCC	O				3 V with fuse controlled by EN VDD video
3	LCDVCC	O				3 V with fuse controlled by EN VDD video
4	+5V	O				+5 V
5	GND	GND				Ground
6	TXCLK-	O				Sampling Clock (Positive : -)
7	TCCLK+	O				Sampling Clock (Negative : +)
8	GND	GND				Ground
9	TXOUT0-	O				Transmission Data of Pixels 0 (Negative : -)
10	TXOUT0+	O				Transmission Data of Pixels 0 (Positive : +)
11	GND	GND				Ground
12	TXOUT1-	O				Transmission Data of Pixels 1 (Negative : -)
13	TXOUT1+	O				Transmission Data of Pixels 1 (Negative : +)
14	GND	GND				Ground
15	TXOUT2-	O				Transmission Data of Pixels 2 (Negative : -)
16	TXOUT2+	O				Transmission Data of Pixels 2 (Negative : +)
17	GND	GND				Ground
18	BLADJ	O				Adjust LCD Brightness Signal
19	EN_BKL	O				Enable backlight
20	+5V	O				support to inverter
21	+5V	O				support to inverter
22	COM3_RTS#	O				COM3 Request to send signal
23	COM3_TXD	O				COM3 Transmitted data signal
24	COM3_RXD	O				COM3 Received data signal

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Pin #	Signal name	Power On	S0 State	S3 State	S4 State	Purpose
25	DDCPCLK	O				DDC Clock
26	DDCPDATA	O				DDC Data
27	USBP7-	O	Low	Low	Low	USB Differential Data Minus
28	USBP7+	O	Low	Low	Low	USB Differential Data Plus
29	+5V	O				Supply to touch screen controller
30	+5V	O				Supply to touch screen controller
31	DVMAIN	O				support to inverter
32	DVMAIN	O				support to inverter
33	+3V	O				+3 V
34	+3V	O				+3 V
35	+3V	O				+3 V
36	COM3_DTR#	O				COM3 Data terminal ready signal
37	LCD_SM_DATA	O				For SM bus GPIO controller
38	LCD_SM_CLK	O				For SM bus GPIO controller
39	GND	GND				Ground
40	TXOUTB0-	O				Transmission Data of Pixels 0 (Negative : -)
41	TXOUTB0+	O				Transmission Data of Pixels 0 (Positive : +)
42	GND	GND				Ground
43	TXOUTB1-	O				Transmission Data of Pixels 1 (Negative : -)
44	TXOUTB1+	O				Transmission Data of Pixels 1 (Negative : +)
45	GND	GND				Ground
46	TXOUTB2-	O				Transmission Data of Pixels 2 (Negative : -)
47	TXOUTB2+	O				Transmission Data of Pixels 2 (Negative : +)
48	GND	GND				Ground
49	TXCLKB-	O				Sampling Clock (Positive : -)
50	TCCLKB+	O				Sampling Clock (Negative : +)

- KBD Connector (MiTAC 291000003015)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	KI7	I				KBD matrix
2	KI6	I				KBD matrix
3	KI5	I				KBD matrix
4	KI4	I				KBD matrix
5	KI3	I				KBD matrix
6	KI2	I				KBD matrix
7	KI1	I				KBD matrix
8	KI0	I				KBD matrix
9	KO15	O				KBD matrix
10	KO14	O				KBD matrix
11	KO13	O				KBD matrix
12	KO12	O				KBD matrix
13	KO11	O				KBD matrix
14	KO10	O				KBD matrix
15	KO9	O				KBD matrix
16	KO8	O				KBD matrix
17	KO7	O				KBD matrix
18	KO6	O				KBD matrix
19	KO5	O				KBD matrix
20	KO4	O				KBD matrix
21	KO3	O				KBD matrix
22	KO2	O				KBD matrix
23	KO1	O				KBD matrix
24	KO0	O				KBD matrix

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Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
25	GND	O				Ground
26	EL_VB	O				EL lamp drive
27	EL_VB	O				EL lamp drive
28	EL_VA	O				EL lamp drive
29	EL_VA	O				EL lamp drive
30	LED_KB_PWR	O				LED keyboard power

- SATA HDD Connector (MiTAC 291000025204)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1-4	+19V_HEAT	O				Heater Power
5	HDD_D-					Remote Thermal Negative Input
6	HDD_D+					Remote Thermal Positive Input
7	TEMP_SEN	I				Temperature Sense
8	+5VA	O				Power Supply
9,10,12	+5VS	O				Power Supply
25	SATAHDD_TXN	O				SATA Differential Signal
26	SATAHDD_TXP	O				SATA Differential Signal
29	SATAHDD_RXN	I				SATA Differential Signal
30	SATAHDD_RXP	I				SATA Differential Signal
11,13,18,34-52	GND	GND				Ground
14-17,19-24, 27,28,31-33	NC					

➢ RTC Battery Connector 2-pin Hirose DF13-2P (MiTAC 291000020233)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	+3VA	O				
2	GND	GND				

- The charge function will not support for RTC battery
- The consumption of RTC CMOS memory will be ~3 uA, the calculated life cycle for the RTC battery is no less than 6 years

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➢ PCMCIA Connector (MiTAC 291000251504)

Pin No	Pin Name	Direction	S0 State	S3 State	S4 State	Description
72	B_CAD0					Card Bus address/data bus
70	B_CAD1					Card Bus address/data bus
71	B_CAD2					Card Bus address/data bus
68	B_CAD3					Card Bus address/data bus
69	B_CAD4					Card Bus address/data bus
65	B_CAD5					Card Bus address/data bus
66	B_CAD6					Card Bus address/data bus
63	B_CAD7					Card Bus address/data bus
62	B_CAD8					Card Bus address/data bus
58	B_CAD9					Card Bus address/data bus
60	B_CAD10					Card Bus address/data bus

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Pin No	Pin Name	Direction	S0 State	S3 State	S4 State	Description
56	B_CAD11					Card Bus address/data bus
54	B_CAD12					Card Bus address/data bus
55	B_CAD13					Card Bus address/data bus
52	B_CAD14					Card Bus address/data bus
53	B_CAD15					Card Bus address/data bus
50	B_CAD16					Card Bus address/data bus
30	B_CAD17					Card Bus address/data bus
29	B_CAD18					Card Bus address/data bus
28	B_CAD19					Card Bus address/data bus
27	B_CAD20					Card Bus address/data bus
24	B_CAD21					Card Bus address/data bus
22	B_CAD22					Card Bus address/data bus
20	B_CAD23					Card Bus address/data bus
18	B_CAD24					Card Bus address/data bus
15	B_CAD25					Card Bus address/data bus
13	B_CAD26					Card Bus address/data bus
11	B_CAD27					Card Bus address/data bus
10	B_CAD28					Card Bus address/data bus
8	B_CAD29					Card Bus address/data bus
7	B_CAD30					Card Bus address/data bus
5	B_CAD31					Card Bus address/data bus
61	B_CCBE0#					Card Bus bus commands and byte enables.
49	B_CCBE1#					Card Bus bus commands and byte enables.
31	B_CCBE2#					Card Bus bus commands and byte enables.
16	B_CCBE3#					Card Bus bus commands and byte enables.

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Pin No	Pin Name	Direction	S0 State	S3 State	S4 State	Description
47	B_CPAR					Card Bus bus parity
45	B_CPERR#					Card Bus parity error indicator
42	B_CGNT#					Card Bus bus grant
40	B_CINT#					Card Bus interrupt
34	B_CIRDY#					Card Bus initiator ready
4	B_CCLKRUN#					Card Bus clock run
73	B_CCD1#					Card Bus detect 1
57,26	B_CVS1, B_CVS2					Cars Bus voltage sense 1 and Card Bus detect 2
46	B_CBLOCK#					Card Bus lock
44	B_CSTOP#					Cars Bus stop
41	B_CDEVSEL#					Card Bus device select
35	B_CTRDY#					Card Bus target ready
32	B_CFRAME#					Card Bus cycle frame
23	B_CRST#					Card Bus reset
21	B_CSERR#					Card Bus system error
19	B_CREQ#					Card Bus request
14	B_CAUDIO					Card Bus audio
12	B_CSTSCHG					Card Bus states change
3	B_CCD2#					Card Bus detect 1
36	B_CCLK					Card Bus clock
38,39	CARD_VB					Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
6	B_RSVD/D2					
48	B_RSVD/A18					
64	B_RSVD/D14					
37	VPPBOUT					Switched output that delivers 0 V 3.3 V, 5 V, 12 V, or high impedance to card

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Pin No	Pin Name	Direction	S0 State	S3 State	S4 State	Description
1,9,17,25,33,59,67,74,75	GND					Ground
147	A_CAD0					Card Bus address/data bus
145	A_CAD1					Card Bus address/data bus
146	A_CAD2					Card Bus address/data bus
143	A_CAD3					Card Bus address/data bus
144	A_CAD4					Card Bus address/data bus
140	A_CAD5					Card Bus address/data bus
141	A_CAD6					Card Bus address/data bus
138	A_CAD7					Card Bus address/data bus
137	A_CAD8					Card Bus address/data bus
133	A_CAD9					Card Bus address/data bus
135	A_CAD10					Card Bus address/data bus
131	A_CAD11					Card Bus address/data bus
129	A_CAD12					Card Bus address/data bus
130	A_CAD13					Card Bus address/data bus
127	A_CAD14					Card Bus address/data bus
128	A_CAD15					Card Bus address/data bus
125	A_CAD16					Card Bus address/data bus
105	A_CAD17					Card Bus address/data bus
104	A_CAD18					Card Bus address/data bus
103	A_CAD19					Card Bus address/data bus
102	A_CAD20					Card Bus address/data bus
99	A_CAD21					Card Bus address/data bus
97	A_CAD22					Card Bus address/data bus
95	A_CAD23					Card Bus address/data bus
93	A_CAD24					Card Bus address/data bus

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Pin No	Pin Name	Direction	S0 State	S3 State	S4 State	Description
90	A_CAD25					Card Bus address/data bus
88	A_CAD26					Card Bus address/data bus
86	A_CAD27					Card Bus address/data bus
85	A_CAD28					Card Bus address/data bus
83	A_CAD29					Card Bus address/data bus
82	A_CAD30					Card Bus address/data bus
80	A_CAD31					Card Bus address/data bus
136	A_CCBE0#					Card Bus bus commands and byte enables.
124	A_CCBE1#					Card Bus bus commands and byte enables.
106	A_CCBE2#					Card Bus bus commands and byte enables.
91	A_CCBE3#					Card Bus bus commands and byte enables.
122	A_CPAR					Card Bus bus parity
120	A_CPERR#					Card Bus parity error indicator
117	A_CGNT#					Card Bus bus grant
115	A_CINT#					Card Bus interrupt
109	A_CIRDY#					Card Bus initiator ready
79	A_CCLKRUN#					Card Bus clock run
148	A_CCD1#					Card Bus detect 1
132,101	A_CVS1, A_CVS2					Cars Bus voltage sense 1 and Card Bus detect 2
121	A_CBLOCK#					Card Bus lock
119	A_CSTOP#					Cars Bus stop
116	A_CDEVSEL#					Card Bus device select
110	A_CTRDY#					Card Bus target ready
107	A_CFRAME#					Card Bus cycle frame

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Pin No	Pin Name	Direction	S0 State	S3 State	S4 State	Description
98	A_CRST#					Card Bus reset
96	A_CSERR#					Card Bus system error
94	A_CREQ#					Card Bus request
89	A_CAUDIO					Card Bus audio
87	A_CSTSCHG					Card Bus states change
78	A_CCD2#					Card Bus detect 2
111	A_CCLK					Card Bus clock
113,114	CARD_VA					Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
81	A_RSVD/D2					
123	A_RSVD/A18					
139	A_RSVD/D14					
112	VPPAOUT					Switched output that delivers 0 V 3.3-V, 5-V, 12-V, or high impedance to card
76,77,84,92,100,108,118,126,134,142,149,150	GND					Ground

- I/O Board 28-pin Connector (Mitac 291000012806)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1-12	NC					Not Connect
19	COM1DCD#	IN				COM1 Carrier detector signal
15	COM1RXD	IN				COM1 Received data signal
27	COM1TXD	O				COM1 Transmitted data signal
23	COM1DTR#	O				COM1 Data terminal ready signal
21	COM1RI#	IN				COM1 Ring indicator signal
17	COM1DSR#	IN				COM1 Data set ready signal
13	COM1RTS#	O				COM1 Request to send signal
25	COM1CTS#	IN				COM1 Clear to send signal
14	MDI0+	I/O				Data Transmit and Receive
16	MDI0-	I/O				Data Transmit and Receive
18	MDI1+	I/O				Data Transmit and Receive
20	MDI1-	I/O				Data Transmit and Receive
22	MDI2+	I/O				Data Transmit and Receive
24	MDI2-	I/O				Data Transmit and Receive
26	MDI3+	I/O				Data Transmit and Receive
28	MDI3-	I/O				Data Transmit and Receive

- I/O Board 120-pin Connector (Mitac 291000011229)-1

Pin #	Signal name	default	S0 State	S3 State	S4 State	Purpose
1	AGND					Analog Ground
2	DEVICE_DECT#					Audio Device detect
3	SPDIFOUT					S/PDIF OUT
4	GND					Ground
5	LCD_SM_DATA					For SM bus GPIO controller
6	LCD_SM_CLK					For SM bus GPIO controller
7	DDCPCLK					DDC Clock
8	DDCPDATA					DDC Data
9	COM3_RXD					COM3 Received data signal
10	COM3_TXD					COM3 Transmitted data signal
11	COM3_RTS#					COM3 Request to send signal
12	SUSB#					S3 control
13-20	PIO_PD0-7					PIO Data bit0~7 signal
21	PIO_STROBE#	O				PIO Strobe
22	PIO_ALF#	O				PIO Auto Feed
23	PIO_ERROR#	I				PIO Printer Error
24	PIO_INIT#	O				PIO Printer Initiate
25	PIO_SLCTIN#	I				PIO printer Select Input
26	PIO_ACK#	I				PIO Printer Acknowledge
27	PIO_BUSY	I				PIO Printer Busy
28	PIO_PE	I				PIO Printer Paper End
29	PIO_SLCT	I				PIO Printer Selected Status
30	LID#					LID Function
31	COM3_DTR#					COM3 Data terminal ready
32-33	+5V					Power Supply
34	CRT_HSYNC					CRT Horizontal Sync. Signal
35	CRT_VSYNC					CRT Vertical Sync. Signal

- I/O Board 120-pin Connector (Mitac 291000011229)-2

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Pin #	Signal name	default	S0 State	S3 State	S4 State	Purpose
36	CRT_DDCCLK					CRT DDC Clock Signal
37	CRT_DDCDATA					CRT DDC Data Signal
38	CRT_BLUE					CRT BLUE Signal
39	CRT_GREEN					CRT GREEN Signal
40	CRT_RED					CRT RED Signal
41	USBP7-	I/O				USB Differential Data Minus
42	USBP7+	I/O				USB Differential Data Plus
43	EN_BKL	O				Enable Backlight
44	BLADJ	O				Adjust LCD Brightness Signal
45-47	LCD_+3VS	O				+3VS For LCD
48	NC					Not Connect
49	GND	GND				Ground
50	TXCLK-					Sampling Clock (Positive : -)
51	TXCLK+					Sampling Clock (Positive : +)
52	GND	GND				Ground
53	TXOUT0-					Transmission Data of Pixels 0 (Negative : -)
54	TXOUT0+					Transmission Data of Pixels 0 (Positive : +)
55	GND	GND				Ground
56	TXOUT1-					Transmission Data of Pixels 1 (Negative : -)
57	TXOUT1+					Transmission Data of Pixels 1 (Positive : +)
58	GND	GND				GROUND
59	TXOUT2-					Transmission Data of Pixels 2 (Negative : -)
60	TXOUT2+					Transmission Data of Pixels 2 (Positive : +)
61,65	AGND					Analog Ground
62	LINE_OUT_L					Audio Line out left signal
63	LINE_OUT_R					Audio Line out right signal
64	MIC					Microphone Input Signal
66-81	KO0-15	O				KBD matrix

- I/O Board 120-pin Connector (Mitac 291000011229)-3

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Pin #	Signal name	default	S0 State	S3 State	S4 State	Purpose
82-89	KI7-0	I				KBD matrix
90	POWERSW#	I				Power Button
91	KBD_EN_EL	O				Keyboard Enable EL
92-93	+3VS	O				Power Supply
94-95	+5VS	O				Power Supply
96-97	+3V	O				Power Supply
98-99	LCD_DVMAIN	O				Power Supply
100	CRT_IN#	I				Indication for CRT IN
101	WLAN_ACTIVE	O				WLAN Communication with BT
102	BT_ACTIVE	I				BT Communication with WLAN
103-108	NC					Not Connect
109	GND					Ground
110	TXOUTB0-					Transmission Data of Pixels 0 (Negative : -)
111	TXOUTB0+					Transmission Data of Pixels 0 (Positive : +)
112	GND					Ground
113	TXOUTB1-					Transmission Data of Pixels 1(Negative : -)
114	TXOUB1+					Transmission Data of Pixels 1(Positive : +)
115	GND					Ground
116	TXOUTB2-					Transmission Data of Pixels 2 (Negative : -)
117	TXOUTB2+					Transmission Data of Pixels 2 (Positive : +)
118	GND					Ground
119	TXCLKB-					Sampling Clock (Positive : -)
120	TXCLKB+					Sampling Clock (Positive : +)

- IDE 50-Pin Connector (MiTAC 291000025038)-1

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	CD_R					CD ROM Audio right Output
2	CD_L					CD ROM Audio left Output
3	GND					Ground
4	CD_COMM					CD ROM Audio ground
5	IDE_PDD8	I/O				IDE Device data 8
6	IDE_RESET	I				Reset
7	IDE_PDD9	I/O				IDE Device data 9
8	IDE_PDD7	I/O				IDE Device data 7
9	IDE_PDD10	I/O				IDE Device data 10
10	IDE_PDD6	I/O				IDE Device data 6
11	IDE_PDD11	I/O				IDE Device data 11
12	IDE_PDD5	I/O				IDE Device data 5
13	IDE_PDD12	I/O				IDE Device data 12
14	IDE_PDD4	I/O				IDE Device data 4
15	IDE_PDD13	I/O				IDE Device data 13
16	IDE_PDD3	I/O				IDE Device data 3
17	IDE_PDD14	I/O				IDE Device data 14
18	IDE_PDD2	I/O				IDE Device data 2
19	IDE_PDD15	I/O				IDE Device data 15
20	IDE_PDD1	I/O				IDE Device data 1
21	IDE_PDDREQ	I				DMA Request
22	IDE_PDD0	I/O				IDE Device data 0
23	IDE_PDIOR#	I				Read Strobe
24-25	GND					Ground
26	IDE_PDIOW	O				Write Strobe
27	IDE_PDDACK#	O				DMA Acknowledge

- IDE 50-Pin Connector (MiTAC 291000025038)-2

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Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
28	IDE_PIORDY	I				I/O Ready
29	NC					Not Connect
30	IDE_IRQ14	O				Interrupt signal
31	CD_DIAG	I/O				Passed Diagnostics
32	IDE_PDA1	O				Address 1
33	IDE_PDA2	O				Address 2
34	IDE_PDA0	O				Address 0
35	IDE_PDCS#3	O				Chip Select signal
36	IDE_PDCS#1	O				Chip Select signal
38	CDACTP#					Led driver
37	+5V					+ 5 volts power
39	+5V					+ 5 volts power
40	+5V					+ 5 volts power
41	+5V					+ 5 volts power
42	+5V					+ 5 volts power
43	GND					Ground
44	GND					Ground
45	NC					Not Connect
46	GND					Ground
47	GND					Ground
48	CSEL					Master device
49	USBP1-	I/O				USB Differential Data Minus
50	USBP1+	I/O				USB Differential Data Plus

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M230 N/B Maintenance

- Speaker Left 2-pin Connector – HIROSE (MiTAC 291000020202)

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1	SPKLOUT+		2W /4 ohm			Line out to speaker left
2	SPKLOUT-		2W /4 ohm			Line out to speaker Left

- PS2 Board 6-pin Connector (MiTAC 291000010630)

Pin #	Signal name	Direction	S0 State	S3 State	S4 State	Purpose
1	+5V					+5V POWER
2	M_CLK					Mouse Clock
3	M_DATA					Mouse Data
4	K_CLK					Keyboard Clock
5	K_DATA					Keyboard Data
6	GND					Ground

- X-Bay 84-pin Connector – (Mitac 291000018402)-1

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
1,3,5,7,9,11,13, 15,17,19,21,23, 29,31,33,35,37	NC					Not Connect
2,4,6	Vsys		O			+19V
8,10,12	+5V		O			+5V
14,16	+3V		O			+3V
18,20	+5VS		O			+5VS
22,24	+3VS		O			+3VS
26	+5VA		O			Always +5V
28	+12V		O			+12V
25,27	USB OC#		I			USB Over Current Signal
30	USBP6-	I/O	Low	Low	Low	USB Differential Data 6 Minus
32	USBP6+	I/O	Low	Low	Low	USB Differential Data 6 Plus
34	USBP3-	I/O	Low	Low	Low	USB Differential Data 3 Minus
36	USBP3+	I/O	Low	Low	Low	USB Differential Data 3 Plus
38	PCIE_RXN2	I				PCIE Signal
40	PCIE_RXP2	I				PCIE Signal
42	PCIE_TXN2	O				PCIE Signal
44	PCIE_TXP2	O				PCIE Signal
46	CLK_PCIE					PCIE Signal
48	CLK_PCIE					PCIE Signal
50	PCIECLKREQ#	I				PCIE Signal
52	PCIE_WAKE#					PCIE Signal
54	PCI_RESET#					PCI Signal

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- X-Bay 84-pin Connector – (Mitac 291000018402)-2

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
56	SMBCLK					SM BUS Clock signal
58	SMBDATA					SMI BUS Data signal
62	MIC					Microphone Input Signal
66	LINEIN_L					Audio Line out left signal
70	LINEIN_R					Audio Line out right signal
74	CCRST					SIM Card Reset Signal
76	CCGND					SIM Card Ground Signal
78	CCIO					SIM Card Serial Data Signal
80	CCVCC					SIM Card Power Signal
82	CCVCC					SIM Card Power Signal
84	CCCLK					SIM Card Clock Signal
39,41,43,45,47, 49,60,64,68,72	GND					Ground
51	SUSB#					S3 control
53	XBAY_GPIO0					GPIO Signal
55	XBAY_GPIO1					GPIO Signal
57	XBAY_RX_YEL					LED Control Signal
59	XBAY_TX_GRN					LED Control Signal
61	XBAY_LINK					LED Control Signal
63	XBAY_ACT					LED Control Signal
65	XBAY_ID0					XBAY ID Select Signal
67	XBAY_ID1					XBAY ID Select Signal
69	COM4_TXD					COM4 Transmitted data signal

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- X-Bay 84-pin Connector – (Mitac 291000018402)-3

Pin #	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Purpose
71	COM4_RXD					COM4 Received data signal
73	COM4_DTR#					COM4 Data terminal ready signal
75	COM4_DCD#					COM4 Carrier detector signal
77	COM4_RTS#					COM4 Request to send signal
79	COM4_CTS#					COM4 Clear to send signal
81	COM4_DSR#					COM4 Data set ready signal
83	COM4_RI#					COM4 Ring indicator signal

1.3 Electrical Characteristic

1.3.1 Keyboard Controller GPIO Pin Definition-1

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
1	/RES	H8_RESET#	I				Reset button	When pin low, the chip is reset/Hardware reset button used
2	XTAL	XTAL	I				Crystal	Clock pulse generator/Using 10MHz input
3	EXTEL	EXTAL	I				Crystal	
4	VCCB	VCCB	I				VDD5	Always 5 V supply
5	MD1	H8_MODE1	I					Set the operating mode/Mode 3 choose single mode
6	MD0	H8_MODE0	I					
7	/NMI	H8_SUSB	I				ICH7-M	S3 control
8	/STBY/FVPP	H8_STBY#	I					standby mode/Always pull high
9	VCC1	VCC1	I				VDD3	Always 3V supply
10	PA7/KEYIN15	K_DATA	O				P/S 2	PA7 input and output pins/ ps2 keyboard data
11	PA6/KEYIN14	K_CLK	O				P/S 2	PA6 input and output pins/ ps2 keyboard clock input and output pins
12	P52/SCK0	BAT_CLK_H8	I/O				Battery	I2C bus clock input and output pins/I2C bus clock output pin
13	P51/RXD0	USE_A	I/O					GPIO/ Software control charger to main or second battery charging
14	P50/TXD0	USE_B	I/O					
15	VSS4	VSS4	I				GND	Ground
16	P97/WAIT/ SDA	BAT_DATA_H8	I				Battery	I2C data input and output pins/I2C data input and output

1.3.1 Keyboard Controller GPIO Pin Definition-2

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
17	P96/0	G_SENSOR#	O				G-sensor	GPI/ HDD drop sensor interrupt pin
18	P95/AS	H8_SB_PWRBTN#	O				ICH7-M	GPIO/ ICH6 power button signal
19	P94/WR	BAT_SM_SW	O					GPIO/ Software control SMBus switch
20	PA5/KEYIN13	M_DATA	O				P/S 2	PA5 input and output pins/ ps2 mouse data input and output pins
21	PA4/KEYIN12	M_CLK	O				P/S 2	PA4 input and output pins/ ps2 mouse clock input and output pins
22	P93/RD	H8_THRM#	O				ICH7-M	GPIO/ Throttle signal
23	P92/IRQ0	H8_LID#	I					GPIO/ LID switch signal input pin
24	P91/IRQ1/EIOW	H8_POWERBTN#	I				Power switch	GPIO/ Power button used
25	P90/IRQ2/ESC2	H8_SUSC	I				ICH7-M	S4 control
26	P60/KEYIN0/FTC1	KBD_KI0	I				Keyboard	Keyboard Matrix
27	P61/KEYIN1/FTOA	KBD_KI1	O				Keyboard	Keyboard Matrix
28	P62/KEYIN2/FTIA	KBD_KI2	I				Keyboard	Keyboard Matrix
29	P63/KEYIN3/FTIB	KBD_KI3	I				Keyboard	Keyboard Matrix
30	PA3/KEYIB11	TPD_DATA	O				Touch Pad	Touch Pad data
31	PA2/KEYIN10	TPD_CLK	O				Touch Pad	Touch Pad clock
32	P64/KEYIN4/FTIC	KBD_KI4	I				Keyboard	Keyboard Matrix
33	P65/KEYIN5/FTID	KBD_KI5	I				Keyboard	Keyboard Matrix
34	P66/KEYIN6/IRQ6	KBD_KI6	O				Keyboard	Keyboard Matrix
35	P67/KEYIN7/IRQ7	KBD_KI7	I				Keyboard	Keyboard Matrix
36	AVREF	AVREF	I				+3VA	Always 3V supply
37	AVCC	AVCC	I				+3VA	Always 3V supply
38	P70/AN0	VBATT1	I				Battery1	Analog input pin/Read main battery voltage

1.3.1 Keyboard Controller GPIO Pin Definition-3

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
39	P71/AN1	VBATT2	I				Battery2	Analog input pin/Read second battery voltage
40	P72/AN2	WAKE_ON_LAN#	I				BCM5752	Wake from LAN
41	P73/AN3	SEN_DDR	I				+1.8V	Analog input pin/Read 1.8V voltage
42	P74/AN4	SEN_3V	I				+3V	Analog input pin/Read 3 V voltage
43	P75/AN5	SEN_VCORE	I				Vcore	Analog input pin/Read Vcore voltage
44	P76/AN6/DA0	ISET	I					Analog output pin/output charger current
45	P77/AN7/DA1	BLADJ	I				Inverter	Analog output pin/LCD panel brightness
46	AVSS	AVSS	I				GND	Ground
47	PA1/KEYIN9	RING#	O					PA1 input and output pins/ Modem ring signal input
48	PA0/KEYIN8	ADEN#	O					PA0 input and output pins/ AC input signal
49	P40/TMCI0	PWROK	I				ICH7-M	GPIO/ Power OK signal output
50	P41/TMO0	SPK_OFF	O				ALC260	GPIO/Software control speaker on or off
51	P42/TMRI0	H8_SMB_DATA	I					I2C bus data input and output pins/I2C bus data input and output pins
52	P43/TMCI1/HIRQ1	H8_SCI	I				ICH7-M	GPIO/ SCI output pin
53	P44/TMO1/HIRQ1	USB_CTRL	O				MIC2545	GPIO/Software control device power on or off
54	P45/TMRI1/HIRQ1	POWERON CARKEY#	I					GPIO/ IGNITION signal power on
55	P46/PW0	PWR_ON	O					GPIO/Output power on signal
56	P47/PW1	HDD_HEAT_PWM	O				HDD	PWM D/A pulse output pin/HDD heater PWM output

1.3.1 Keyboard Controller GPIO Pin Definition-4

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
57	PB7/XDB7	LED_DATA	I/O				LED	PB7 input and output pins/ Output LED indicator data signal
58	PB6/XDB6	LED_CLK	I/O				LED	PB6 input and output pins/ Output LED indicator clock signal
59	VCC2	VCC2	I				+3VA	Always 3V supply
60	P27/A15	KO15	O				Keyboard	Keyboard Matrix
61	P26/A14	KEY BD MATRIX : KO14	O				Internal Keyboard	Keyboard Matrix
62	P25/A13	KEY BD MATRIX : KO13	O				Internal Keyboard	Keyboard Matrix
63	P24/A12	KEY BD MATRIX : KO12	O				Internal Keyboard	Keyboard Matrix
64	P23/A11	KEY BD MATRIX : KO11	O				Internal Keyboard	Keyboard Matrix
65	P22/A10	KEY BD MATRIX : KO10	O				Internal Keyboard	Keyboard Matrix
66	P21/A9	KEY BD MATRIX : KO9	O				Internal Keyboard	Keyboard Matrix
67	P20/A8	KEY BD MATRIX : KO8	O				Internal Keyboard	Keyboard Matrix
68	PB5/XDB4	ALERT	I/O				Battery	PB5 input and output pins
69	PB4/XDB4	LEARNING#	I/O				Battery	disable AC function
70	VSS1	VSS1	I				GND	Ground
71	VSS2	VSS2	I				GND	Ground
72	P17/A7	KEY BD MATRIX : KO7	O				Internal Keyboard	Keyboard Matrix
73	P16/A6	KEY BD MATRIX : KO6	O				Internal Keyboard	Keyboard Matrix

1.3.1 Keyboard Controller GPIO Pin Definition-5

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
74	P15/A5	KEY BD MATRIX : KO5	O				Internal Keyboard	Keyboard Matrix
75	P14/A4	KEY BD MATRIX : KO4	O				Internal Keyboard	Keyboard Matrix
76	P13/A3	KEY BD MATRIX : KO3	O				Internal Keyboard	Keyboard Matrix
77	P12/A2	KEY BD MATRIX : KO2	O				Internal Keyboard	Keyboard Matrix
78	P11/A1	KEY BD MATRIX : KO1	O				Internal Keyboard	Keyboard Matrix
79	P10/A0	KEY BD MATRIX : KO0	O				Internal Keyboard	Keyboard Matrix
80	PB3/XDB3	BAT2_IN#	I/O				Battery	PB3 input and output pins/second battery plug in signal
81	PB2/XDB2	RCIN#	I/O				ICH7-M	PB2 input and output pins/ Reset CPU signal
82	P30/HDB0/D0	LPC_LAD0	I/O					LPC command, address, data input and output pins/LPC address and data input and output
83	P31/HDB1/D1	LPC_LAD1	I/O					
84	P32/HDB2/D2	LPC_LAD2	I/O					
85	P33/HDB3/D3	LPC_LAD3	I/O					
86	P34/HDB4/D4	FRAME#	I/O					The start of an LPC cycle or forced termination of an abnormal LPC cycle/LPC frame
87	P35/HDB5/D5	PLT_RST#	I/O					LPC reset/LPC reset
88	P36/HDB6/D6	PCI_H8_CLK	I/O				Clock	LPC clock input pin/LPC clock
89	P37/HDB7/D7	SERIRQ	I/O				ICH7-M	Input and output pin for LPC serialized host interrupts/LPC serial host interrupts

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1.3.1 Keyboard Controller GPIO Pin Definition-6

PIN	Port	Signal name	Power On default Direction	S0 State	S3 State	S4 State	Connect to	Description
90	PB1/XDB1	DOCK_IN#	I/O				Docking	LSCI output pin/ Dock in signal input
91	PB0/XDB0	EXTSMI#	I/O				ICH7-M	LSMI output pin/SMI output pin
92	VSS3	VSS3	I				GND	Ground
93	P80/HA0	IDE_HDD_PWR	I/O				HDD	GPIO/ HDD power on or off
94	P81/GA20	A20GATE	I/O				ICH7-M	A20 gate control signal output pin/A20 gate used
95	P82/CLKRUN#	PCI_CLKRUN	I/O				PCI device	Input and output pins that requests the start of LCLK operation when LCLK is stopped/LCLK function used
96	P83/PLCPD#	LPC_PD#	I/O					Input pin that controls LPC module shutdown/controls LPC module shutdown
97	P84/IRQ2/TXD1	H8_WAKE_UP#	I					GPIO/Wakeup event
98	P85/IRQ4/RXD1	RSMRST#	I					Resume reset
99	P86/IRQ5/SCK1	H8_SMB_CLjK	I					I2C bus clock input and output pins/I2C bus clock output pin
100	/RESO	N/A	O					

1.3.2 ICH7-M GPIO Pin Definition-1

Item	Multi. Func./Note	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
0	PM_BMBUSY#	GPIO0	I		Low	Low	Core
1	PCI_REQ5#(Reserved)	GPIO1/REQ5#	I		Low	Low	Core
2	PCI_INTE#	GPIO2/PIRQE#	I		Off	Off	Core
3	PCI_INTF#	GPIO3/PIRQF#	I		Off	Off	Core
4	PCI_INTG#	GPIO4/PIRQG#	I		Off	Off	Core
5	PCI_INTH#	GPIO5/PIRQH#	I		Off	Off	Core
6	GPO_ENOVA	GPIO6	I		Off	Off	Core
7	SCI#	GPIO7	I		Off	Off	Core
8	EXTSMI#	GPIO8	I		Driven	Driven	Resume
9	SUSPEND#	GPIO9	I		Driven	Driven	Resume
10	XBAY_GPIO0	GPIO10	I		Driven	Driven	Resume
11	SMBALERT#	GPIO11/SMBALERT#	Native		Driven	Driven	Resume
12	T/P	GPIO12	I		Driven	Driven	Resume
13	XBAY_GPIO1	GPIO13	I		Driven	Driven	Resume
14	KBD_EN_EL	GPIO14	I		Driven	Driven	Resume
15	IDE_HDD_RST#	GPIO15	I		Driven	Driven	Resume
16	DPRSLPVR	GPIO16/DPRSLPVR	Native		Off	Off	Core
17	PCI_GNT5#	GPIO17/GNT5#	O		Off	Off	Core
18	STOP_PCI#	GPIO18/STPPCI#	O		Off	Off	Core
19	XBAY_ID0	GPIO19/STA1GP	I		Off	Off	Core
20	STOP_CPU#	GPIO20/STPCPU#	O		Off	Off	Core
21	T/P	GPIO21/STA0GP	I		Driven		Core
22	PCI_REQ4#	GPIO22/REQ4#	Native		Low	Low	Core
23	LDRQ#1	GPIO23	Native		Low	Low	Core

1.3.2 ICH7-M GPIO Pin Definition-2

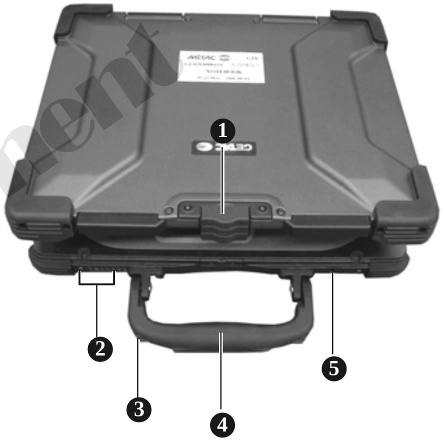
Item	Multi. Func./Note	Signal Name / Description	Power On default Direction	S0 State	S3 State	S4 State	Power plane
24	GPO_ENOVA1	GPIO24	O		Defined	Defined	Resume
25	GPO_ENOVA2	GPIO25	O		Defined	Defined	Resume
26	T/P	GPIO26/EL_RSVD	O		Defined	Defined	Resume
27	T/P	GPIO27/EL_STATE0	O		Defined	Defined	Resume
28	T/P	GPIO28/EL_STATE0	O		Defined	Defined	Resume
29	USBOC#5	GPIO29	Native		Driven	Driven	Resume
30	USBOC#6	GPIO30	Native		Driven	Driven	Resume
31	USBOC#7	GPIO31	Native		Driven	Driven	Resume
32	PCI_CLKRUN#	GPIO32	O				Core
33	MINI_PD#	GPIO33	O		Off	Off	Core
34	ENABKL_SB	GPIO34	O		Off	Off	Core
35	SATACLKREQ#	GPIO35	O		Off	Off	Core
36	T/P	GPIO36	I		Driven		Core
37	XBAY_ID1	GPIO37	I		Off	Off	Core
38	CRT_IN#	GPIO38	I		Off	Off	Core
39	KBD_US/JP#	GPIO39	I		Off	Off	Core
40	NOT Implemented	GPIO40~47	implemented				N/A
41	PCI_GNT4#	GPIO48	Native		Off	Off	Core
42	HPWRGD	GPIO49	Native		Off	Off	CPU_IO
43							

2. System View and Disassembly

2.1 System View

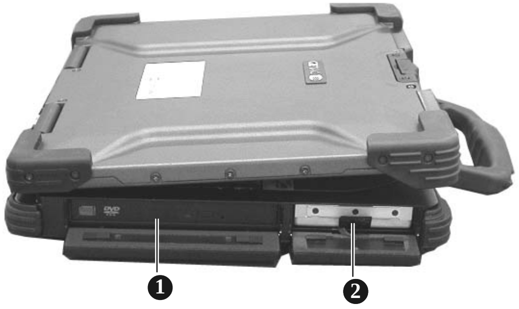
2.1.1 Front View

- ❶ Top Cover Latch
- ❷ Device Indicators
- ❸ Touch Screen Pen
- ❹ Handle
- ❺ Kensington Lock



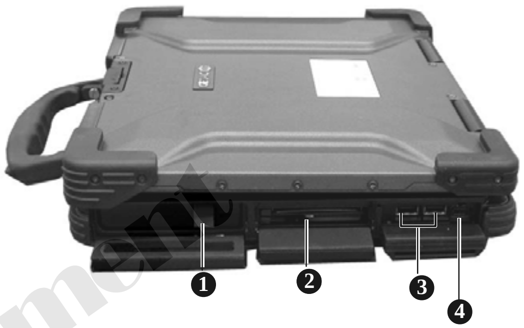
2.1.2 Left-side View

- ❶ CD/Combo/DVD RW Drive
- ❷ Hard Disk Drive



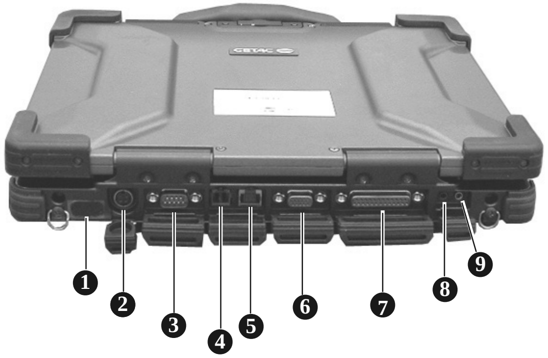
2.1.3 Right-side View

- ❶ Primary Battery Pack
- ❷ PC Card Slot
- ❸ USB Port*2
- ❹ 1394B Port



2.1.4 Rear View

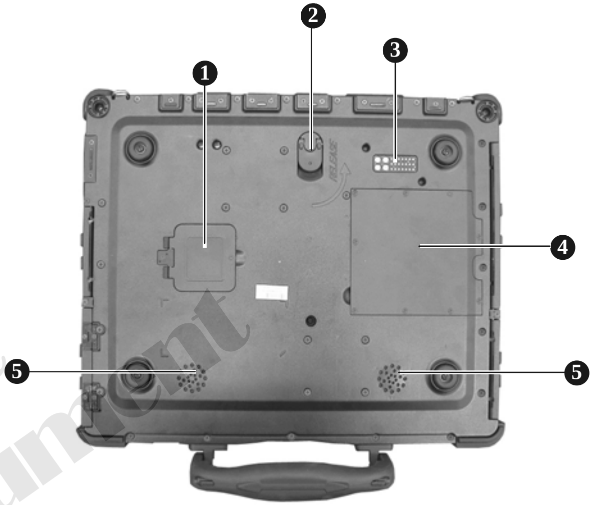
- ❶ IR Port
- ❷ Power Connector
- ❸ Serial Port
- ❹ RJ11 Port
- ❺ RJ45 Port
- ❻ External VGA Port
- ❼ Parallel Port
- ❽ External Microphone Connector
- ❾ Line Out Connector



M230 N/B Maintenance

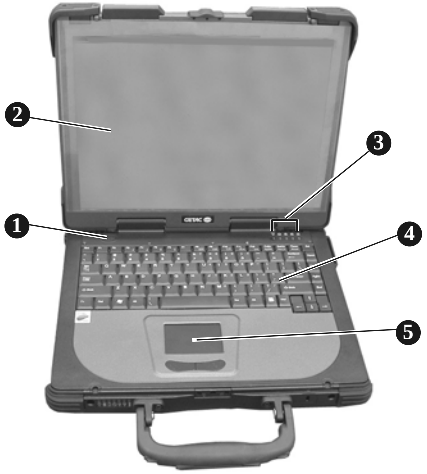
2.1.5 Bottom View

❶ SIM Card Slot
❷ Release Knob
❸ Docking Connector (POGO)
❹ Memory Slot
❺ Stereo Speaker Set



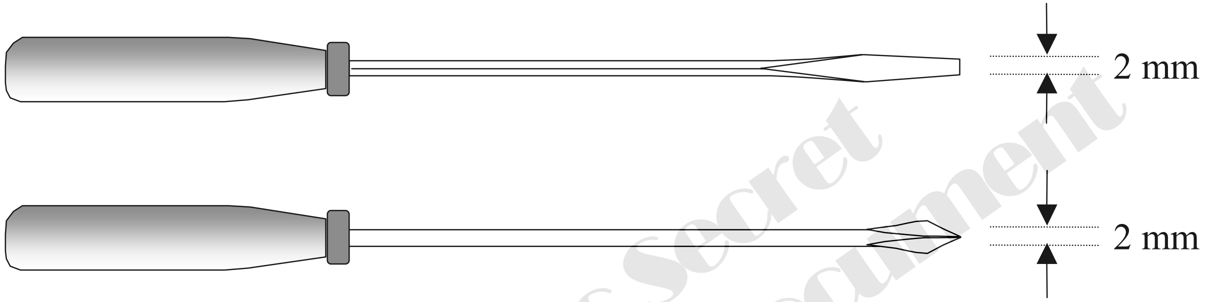
2.1.6 Top-open View

❶ Power Button
❷ LCD Screen
❸ Device Indicators
❹ Keyboard
❺ Touch Pad

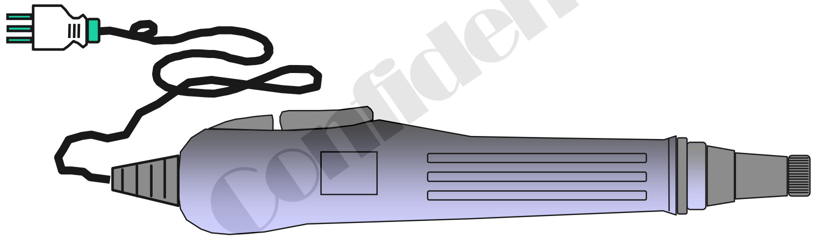


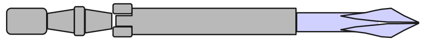
2.2 Tools Introduction

1. Minus screw driver for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.





Bit Size

#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm^2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

- **NOTEBOOK**
  - **Modular Components**
    - **2.3.1 Battery Pack**
    - **2.3.2 HDD Module**
    - **2.3.3 CD-ROM**
    - **2.3.4 Keyboard**
    - **2.3.5 Wireless Card**
    - **2.3.6 DDR2-SDRAM**
  - **LCD Assembly Components**
    - **2.3.7 LCD Assembly**
    - **2.3.8 LCD Panel**
    - **2.3.9 Touch Screen Board**
    - **2.3.10 Inverter Board**
  - **Base Unit Components**
    - **2.3.11 System Board**
    - **2.3.12 Modem Card**

2.3.1 Battery Pack

Disassembly

1. Open the battery door. (Figure 2-1)
2. Pull the battery holder out. (Figure 2-2)

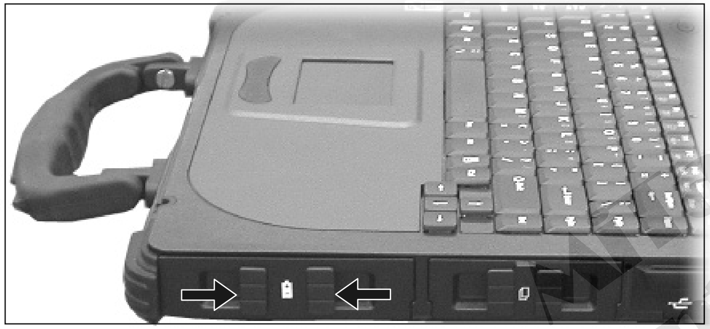


Figure 2-1 Open the battery door

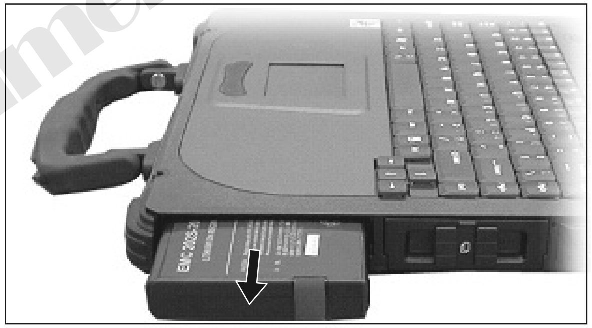


Figure 2-2 Pull the battery holder out

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Reassembly

1. Replace the battery pack into the compartment.
2. Push the battery door inside slightly to close it.

2.3.2 HDD Module

Disassembly

1. Open the HDD door. (Figure 2-3)
2. Pull the HDD out. (Figure 2-4)

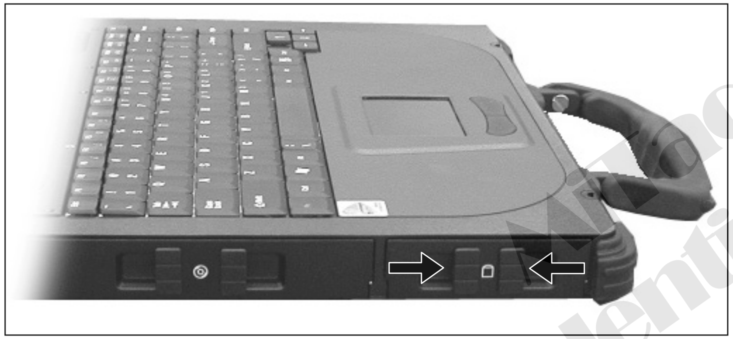

Figure 2-3 Open the HDD door

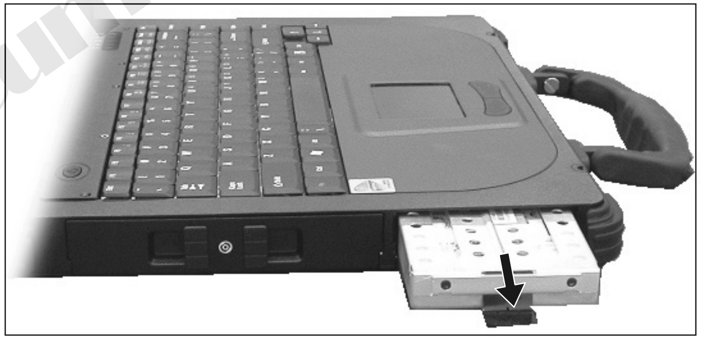

Figure 2-4 Pull the HDD out

Reassembly

1. Replace the HDD into the compartment.
2. Push the HDD door inside slightly to close it.

2.3.3 CD-ROM

Disassembly

1. Open the CD-ROM door. (Figure 2-5)
2. Put the notebook upside down and put the ejector direct. (Figure 2-6)

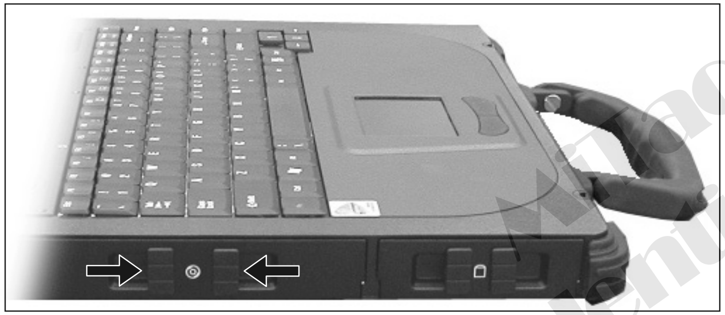

Figure 2-5 Open the CD-ROM door

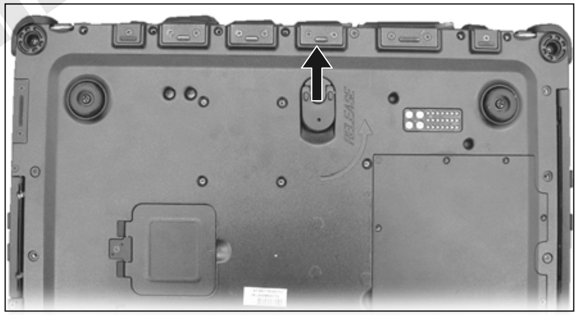

Figure 2-6 Put the ejector direct

3. Turn the ejector counterclockwise to push the CD-ROM out. (Figure 2-7)

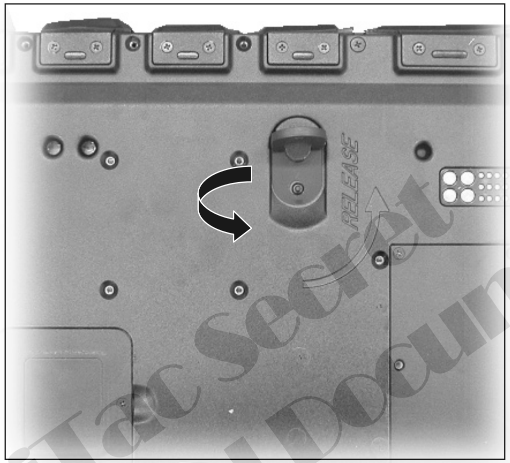

Figure 2-7 Turn the ejector counterclockwise

Reassembly

1. Replace the CD-ROM module into the compartment.
2. Push the CD-ROM door inside slightly to close it.

2.3.4 Keyboard

Disassembly

1. Open the top cover then remove five screws. (Figure 2-8)
2. Turn to back then remove four screws. (Figure 2-9)

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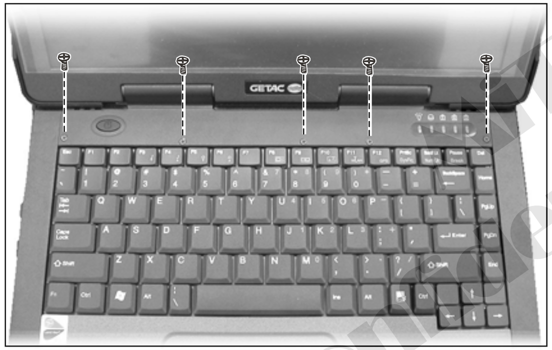

Figure 2-8 Remove five screws

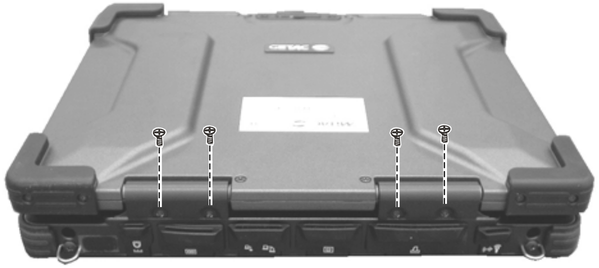

Figure 2-9 Remove four screws

3. Open the top cover to 180-degree then slightly lift up the hinge cover. (Figure 2-10)

4. Remove four screws and open the bracket. (Figure 2-11)

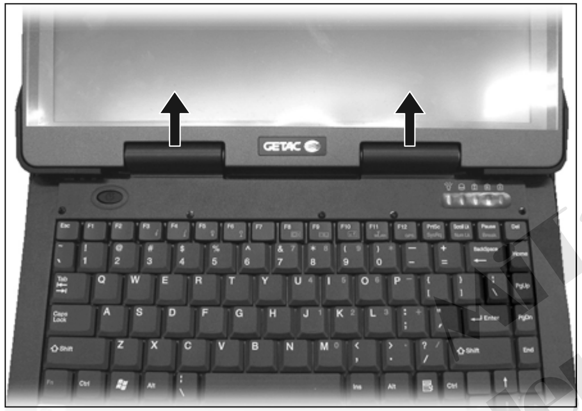

Figure 2-10 Remove the hinge cover

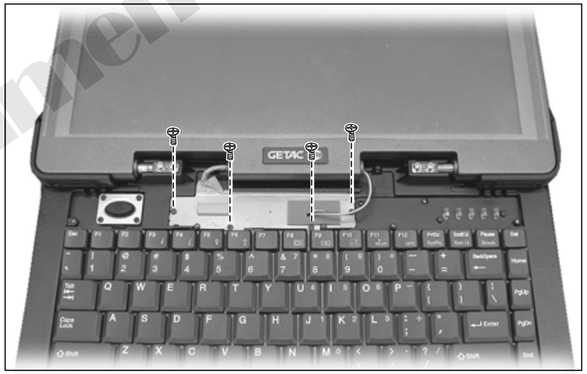

Figure 2-11 Remove four screws

M230 N/B Maintenance

5. Disconnect the keyboard cable. (Figure 2-12)

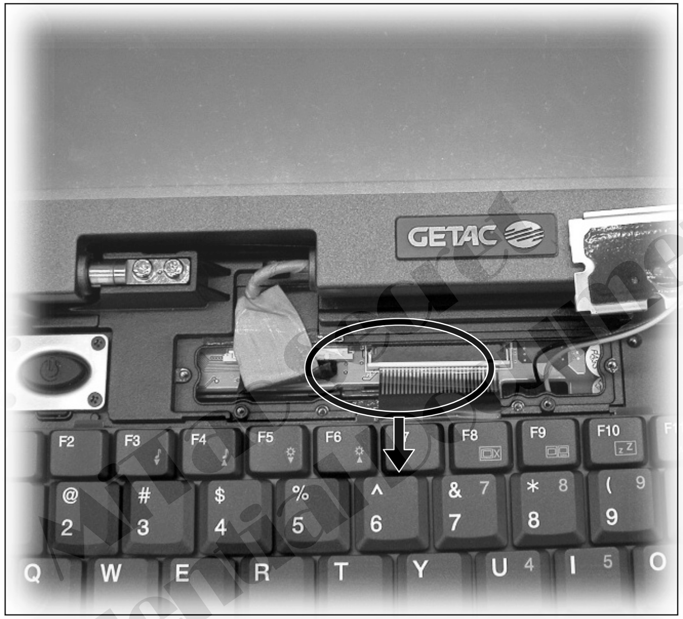

Figure 2-12 Disconnect keyboard cable

Reassembly

1. Reconnect the keyboard cable.
2. Replace the bracket and secure with four screws.
3. Replace the hinge cover and secure with five screws.
4. Turn to back, then secure the hinge cover with four screws.

2.3.5 Wireless Card

Disassembly

1. Remove the battery pack and keyboard. (Refer to section 2.3.1 and 2.3.4 Disassembly)
2. Remove ten screws fastening the LED board cover. (Figure 2-13)
3. Disconnect the LED board's cable. (Figure 2-14)

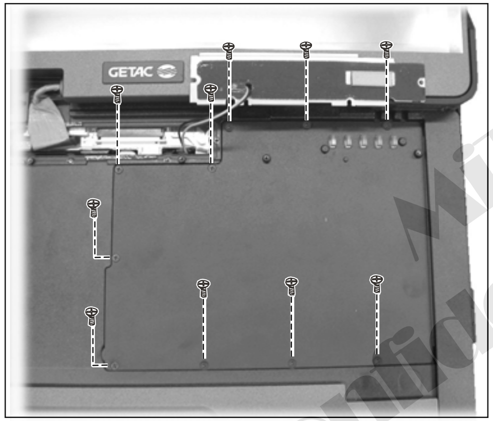

Figure 2-13 Remove ten screws

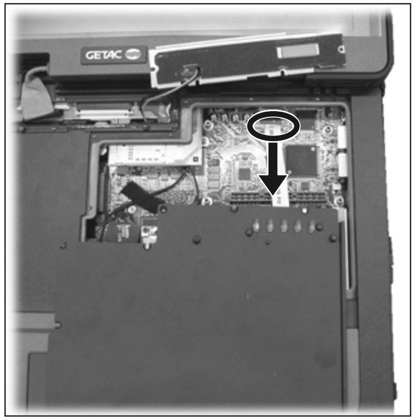

Figure 2-14 Disconnect the LED board's cable

5. Disconnect the wireless card’s antennae first. Then remove two screws and remove the wireless card. (Figure 2-15)

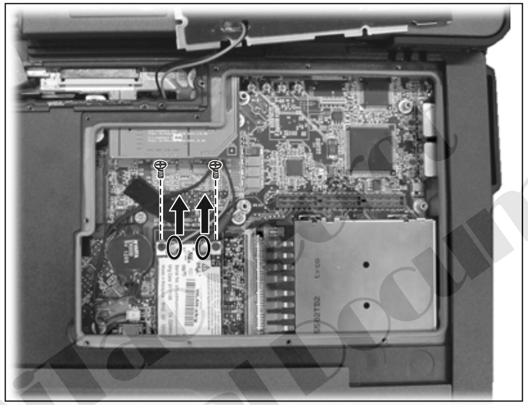

Figure 2-15 Free the wireless card

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Reassembly

1. Replace the wireless card and secure with two screws. Then sure that the antennae fully populated.
2. Replace the LED board’s cable and then secure the LED board cover with ten screws.
4. Replace the keyboard and battery pack. (Refer to sections 2.3.4 and 2.3.1 Reassembly.)

2.3.6 DDR2

Disassembly

1. Remove the battery pack. (Refer to sections 2.3.1 Disassembly)
2. Remove nine screws fastening the DDR2-SDRAM cover. (Figure 2-16)
3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-17)

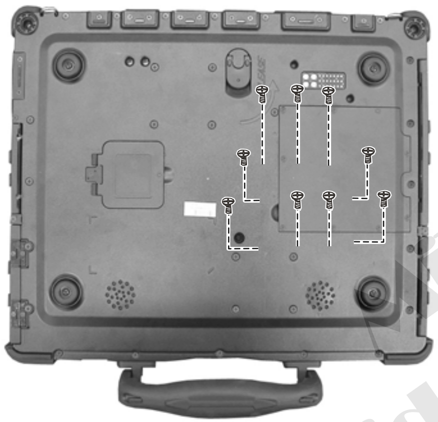

Figure 2-16 Remove nine screws

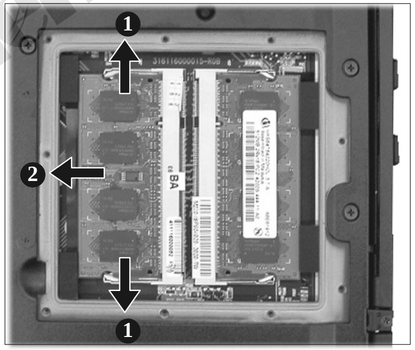

Figure 2-17 Remove the SO-DIMM

Reassembly

1. To install the DDR2, match the DDR2's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at a 20-degree angle. Then push down until the retaining clips lock the DDR2 into position.
2. Replace the DDR2-SDRAM cover and secure with nine screws.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.7 LCD Assembly

Disassembly

1. Remove the battery pack and keyboard. (Refer to section 2.3.1 and 2.3.4 Disassembly)
2. Disconnect the LCD cable from the I/O board. And remove four screws to free the LCD assembly. (Figure 2-18)

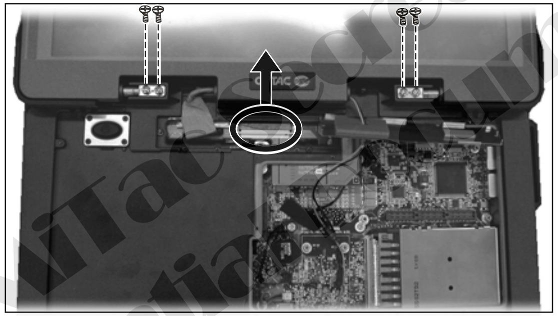

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Figure 2-18 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the LCD cable to the I/O board.
3. Replace the keyboard and battery pack. (Refer to sections 2.3.4 and 2.3.1 Reassembly)

2.3.8 LCD Panel

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.3.1 and 2.3.4 Disassembly)
2. Remove sixteen screws to release four corner rubbers. (Figure 2-19)
3. Remove eight screws. (Figure 2-20)

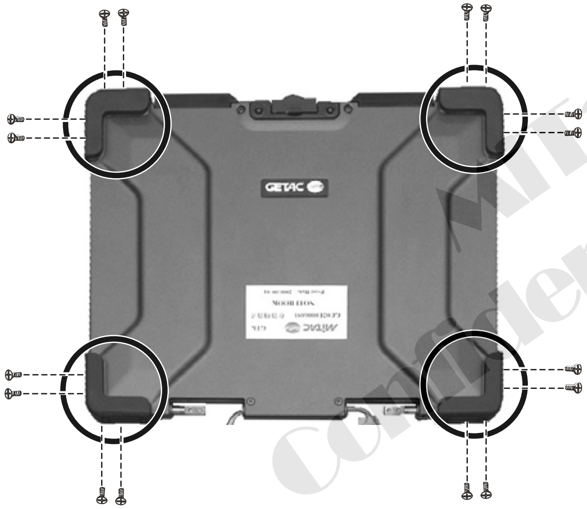

Figure 2-19 Remove four corner rubbers

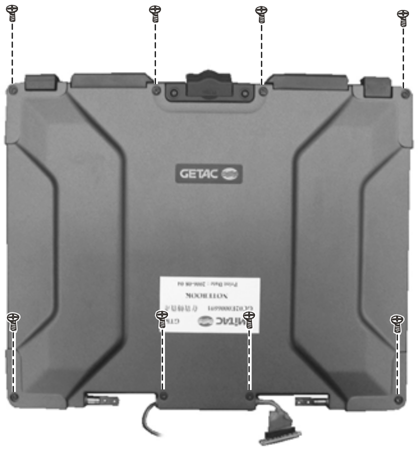

Figure 2-20 Remove eight screws

4. Remove six screws to free the LCD housing. (Figure 2-21)
5. Open the LCD cover carefully. Be careful with the touch screen cable! (Figure 2-22)

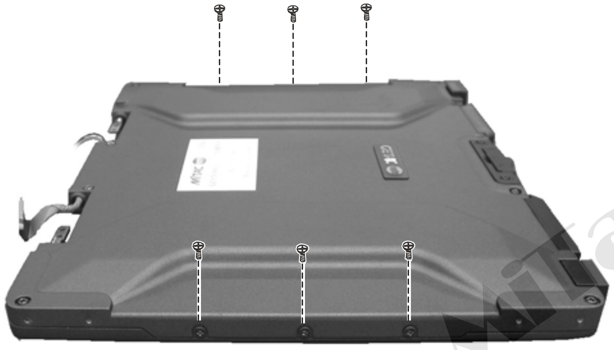

Figure 2-21 Remove six screws

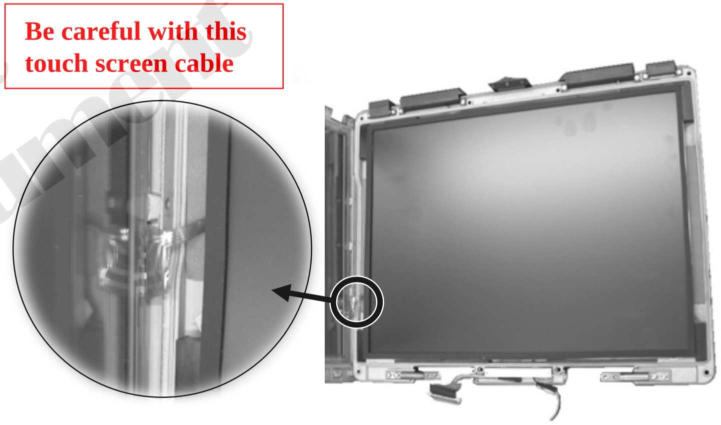
Be careful with this touch screen cable

Figure 2-22 Free the LCD cover

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M230 N/B Maintenance

6. To disconnect the inverter cable, lift the transparent plastic clip up firmly to remove it from the connector(❶). Then disconnect the inverter cable (❷). (Figure 2-23)
7. Disconnect the LCD cable to free the panel. (Figure 2-24)

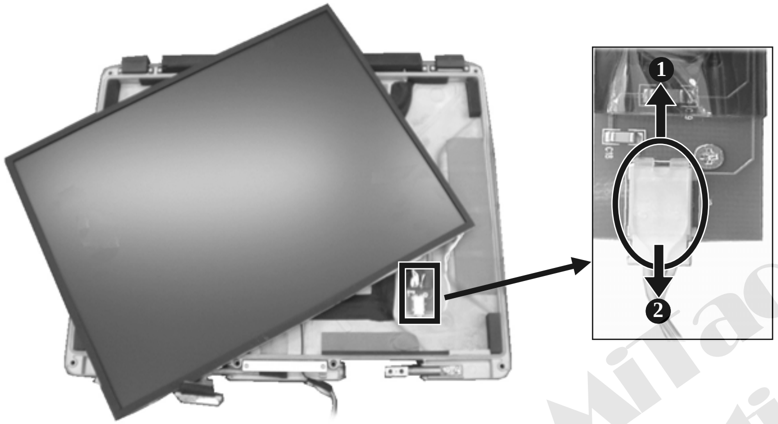

Figure 2-23 Disconnect the inverter cable

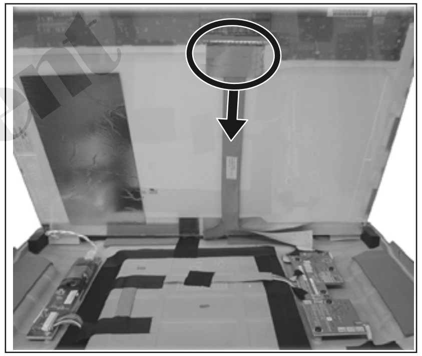

Figure 2-24 Disconnect the LCD cable

Reassembly

1. Reconnect the LCD CABLE, inverter cable and touch screen cable. Then fit the panel.
2. Replace LCD cover. Secure the LCD housing with fourteen screws.
3. Replace four corner rubbers and secure with sixteen screws.
4. Replace the LCD assembly, keyboard and battery pack. (Refer to sections 2.3.7, 2.3.4 and 2.3.1 Reassembly)

2.3.9 Touch Screen Board

Disassembly

1. Remove the battery, keyboard, LCD assembly and LCD panel. (Refer to section 2.3.1, 2.3.4, 2.3.7 and 2.3.8 Disassembly)
2. Remove three screws and disconnect two cables to free the touch screen board. (Figure 2-25)

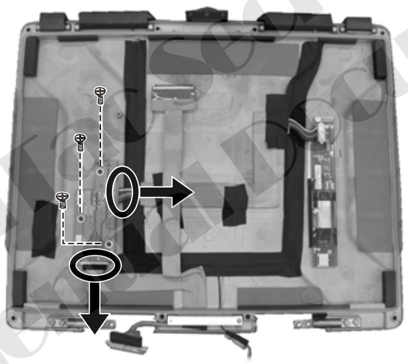

Figure 2-25 Free the touch screen board

Reassembly

1. Fit the touch screen board back into place and secure with three screws. Reconnect two cables.
2. Replace the LCD panel into LCD housing. Then reconnect the touch screen cable and inverter cable.
3. Replace the LCD panel. (Refer to section 2.3.8 Reassembly)
4. Replace the LCD assembly, keyboard and battery pack. (Refer to sections 2.3.7, 2.3.4 and 2.3.1 Reassembly)

2.3.10 Inverter Board

Disassembly

1. Remove the battery, keyboard, LCD assembly and LCD panel. (Refer to section 2.3.1, 2.3.4, 2.3.7 and 2.3.8 Disassembly)
2. Remove two screws and disconnect one cable to free the inverter board. (Figure 2-26)

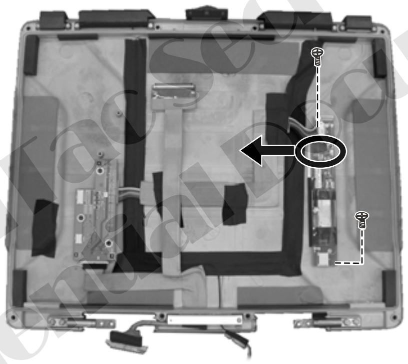

Figure 2-26 Free the inverter board

Reassembly

1. Fit the inverter board back into place and secure with three screws. Reconnect one cable.
2. Replace the LCD panel into LCD housing. Then reconnect the touch screen cable and inverter cable.
3. Replace the LCD panel. (Refer to section 2.3.8 Reassembly)
4. Replace the LCD assembly, keyboard and battery pack. (Refer to section 2.3.7, 2.3.4 and 2.3.1 Reassembly)

2.3.11 System Board

Disassembly

1. Remove the battery, HDD, CD-ROM, keyboard, wireless card, DDR2 and LCD assembly. (Refer to sections 2.3.1~2.3.7 Disassembly)
2. Remove thirty-four screws. (Figure 2-27)
3. Remove six stand-off screws. (Figure 2-28)

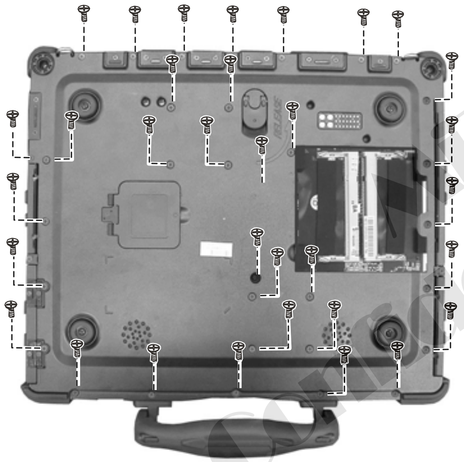

Figure 2-27 Remove thirty-four screws

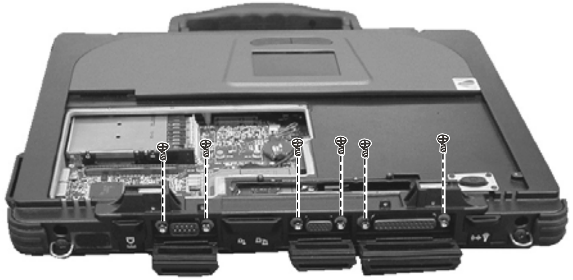

Figure 2-28 Remove sis stand-off screws

M230 N/B Maintenance

4. Remove two speakers’ cables to free the bottom cover. (Figure 2-29)

5. Remove eight screws and disconnect T/P SW wire to free the system board. (Figure 2-30)

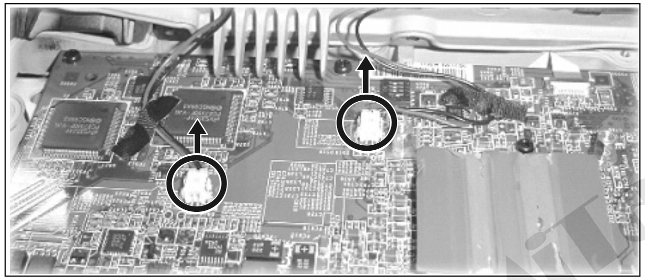

Figure 2-29 Free the bottom cover

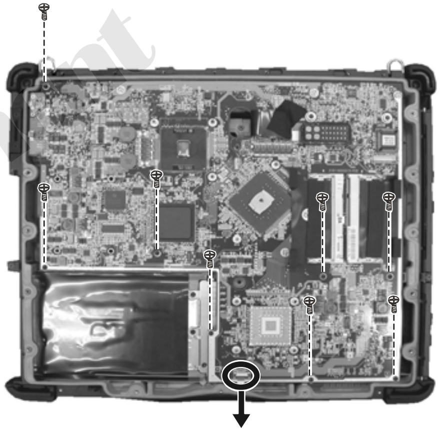

Figure 2-30 Remove eight screws

6. Remove four screws fixing the PCMCIA socket. (Figure 2-31)
7. Turn over, lift the PCMCIA socket straightly to free it from the system board. (Figure 2-32)
8. Turn over the base unit, then lift up the system board from the housing.

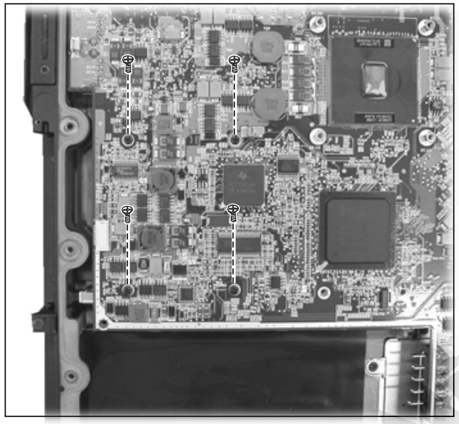

Figure 2-31 Remove four screws

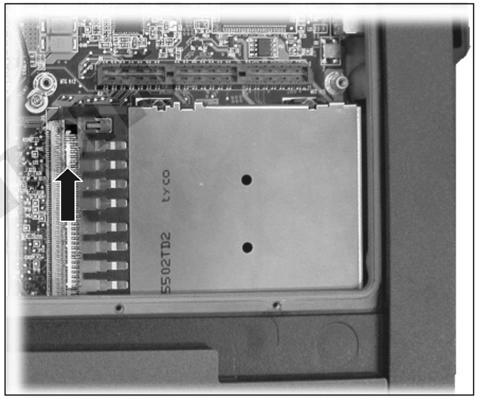

Figure 2-32 Free the PCMCIA socket

Reassembly

1. Put the PCMCIA socket back to its place in the housing.
2. Replace the system board back into the housing. Reconnect the PCMCIA socket to the system board and secure with four screws.
3. Secure the system board with eight screws.
4. Turn over the base unit. Secure with fifteen screws and reconnect one cable.
5. Replace the LCD assembly, DDR2, wireless card, keyboard, CD-ROM, HDD and battery pack. (Refer to the previous sections reassembly)

2.3.12 I/O Board

Disassembly

1. Remove the battery, HDD, CD-ROM, keyboard, wireless card, DDR2, LCD assembly and system board. (Refer to sections 2.3.1~2.3.7, 2.3.11 Disassembly)
2. Remove three screws. (Figure 2-33)
3. Disconnect modem's cable, then free the I/O board. (Figure 2-34)

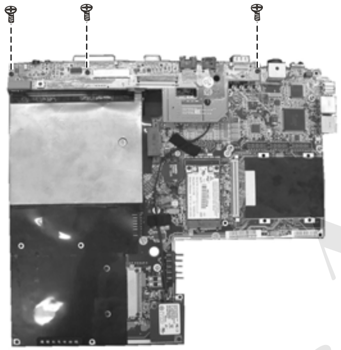

Figure 2-33 Remove three screws

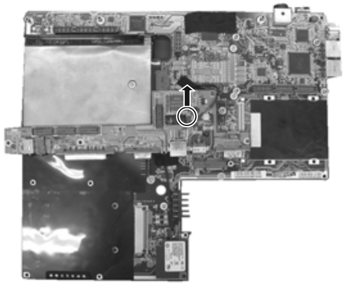

Figure 2-34 Free the I/O board

Reassembly

1. Replace the modem card back into the system board and secure with two screws.
2. Replace the system board, LCD assembly, DDR2, wireless card, keyboard, CD-ROM, HDD and battery pack. (Refer to previous sections Reassembly)

2.3.13 Modem Card

Disassembly

1. Remove the battery, hard disk drive, CD-ROM, keyboard, wireless card, DDR2, LCD assembly, system board and I/O board. (Refer to sections 2.3.1~2.3.7, 2.3.11 and 2.3.12 Disassembly)
2. Remove two screws, then free the modem card. (Figure 2-35)

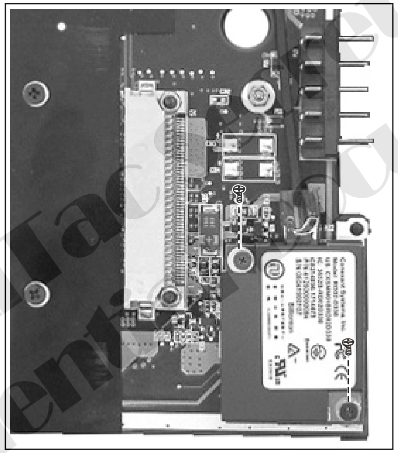

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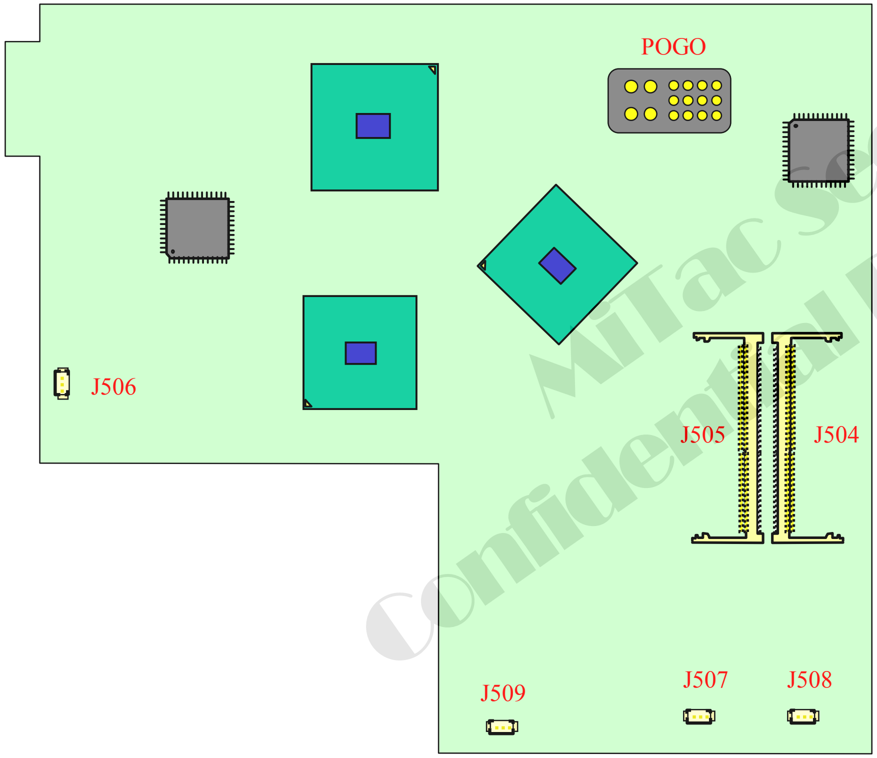
Figure 2-35 Remove the modem card

Reassembly

1. Replace the modem card back into the system board and secure with two screws.
2. Replace the system board, LCD assembly, DDR2, wireless card, keyboard, CD-ROM, HDD and battery pack. (Refer to previous section Reassembly)

3. Definition & Location of Connectors/Switches

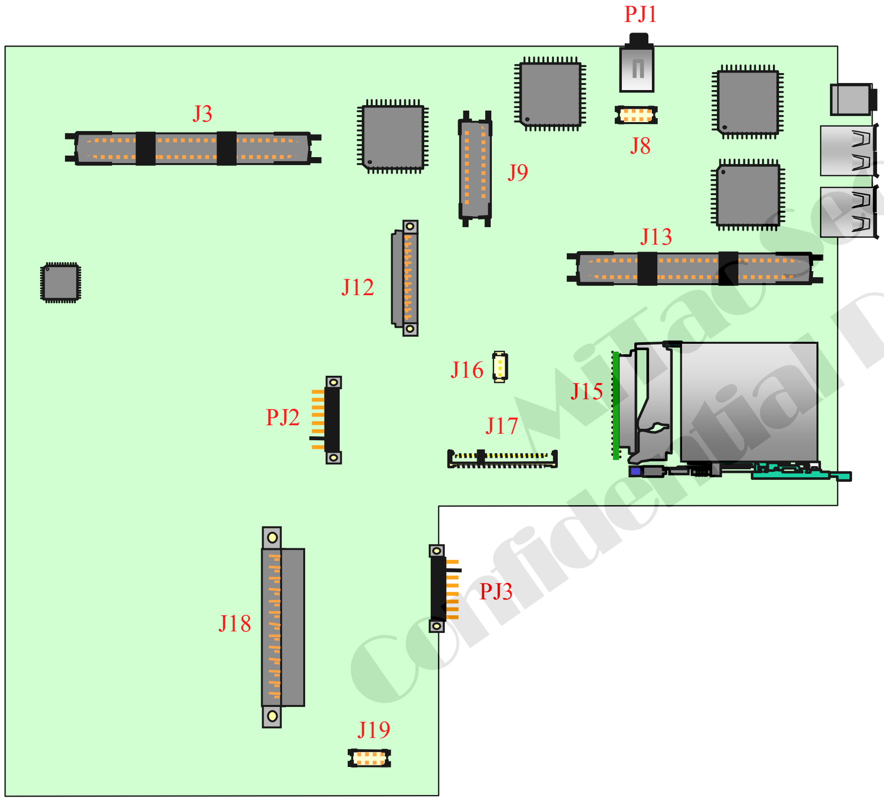
3.1 Mother Board (Side A)


POGO
J506
J505
J504
J509
J507
J508

- **J504, J505: DDR2 SO-DIMM Socket**
- **J506: SIM Interface**
- **J507: Right Audio Channel Connector**
- **J508: Left Audio Channel Connector**
- **J509: Switch Board Cable Connector**

3. Definition & Location of Connectors/Switches

3.1 Mother Board (Side B)


PJ1
J2
J3
J8
J9
J10
J11
J12
J13
J16
J15
PJ2
J17
J18
PJ3
J19

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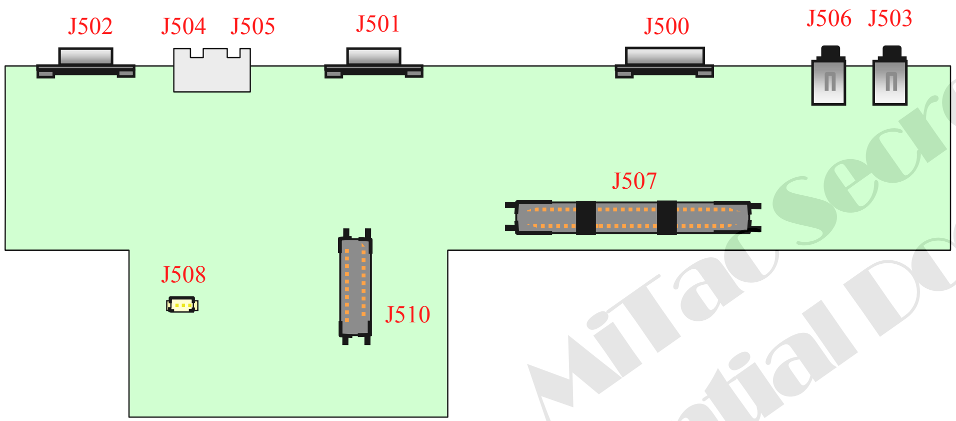
- **J2: 1394b Port**
- **J3: I/O Board Connector**
- **J8: LED Board Connector**
- **J9: COM1&Giga LAN Board Connector**
- **J10, J11: USB Port**
- **J12: CD-ROM Connector**
- **J13: X-BAY Connector**
- **J15: PC Card Slot**
- **J16: CMOS Battery Connector**
- **J17: PCI Express Connector**
- **J18: SATA HDD Connector**
- **J19: MDC Connector**
- **PJ1: Power Jack**
- **PJ2: Secondary Battery Connector**
- **PJ3: Primary Battery Connector**

3. Definition & Location of Connectors/Switches

3.2 I/O Board (Side A)

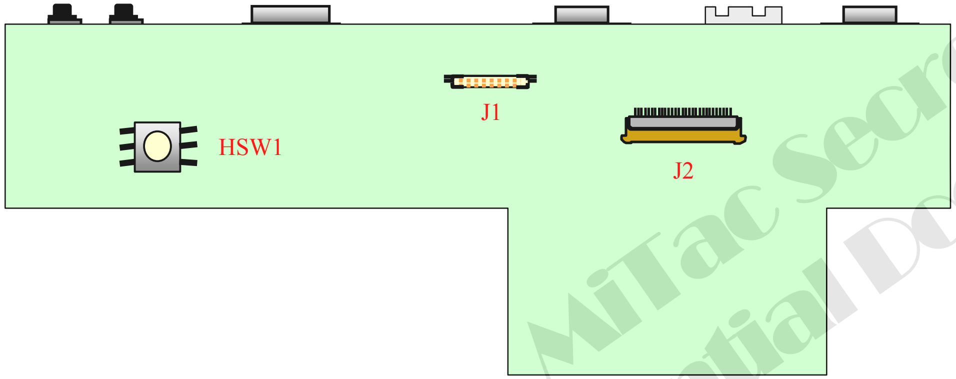

J502
J504
J505
J501
J500
J506
J503
J507
J508
J510

- **J500: Parallel Port**
- **J501: External VGA Connector**
- **J502: Serial Port**
- **J503: External Microphone Jack**
- **J504: RJ11 Connector**
- **J505: RJ45 Connector**
- **J506: Line Out Phone Jack**
- **J507: I./O Board to MB Connector**
- **J508: Modem Jump Wire Connector**
- **J510: COM1&Giga LAN Board Connector**

M230 N/B Maintenance

3. Definition & Location of Connectors/Switches

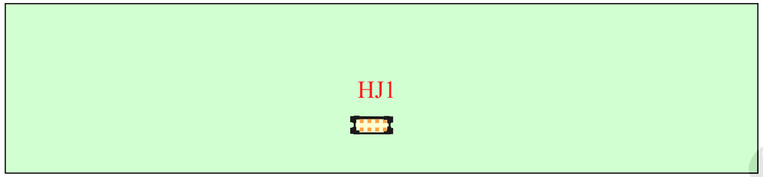
3.2 I/O Board (Side B)



- **J1: LCD Cable Connector**
- **J2: Internal Keyboard Connector**
- **HSW1: Power Button**

3. Definition & Location of Connectors/Switches

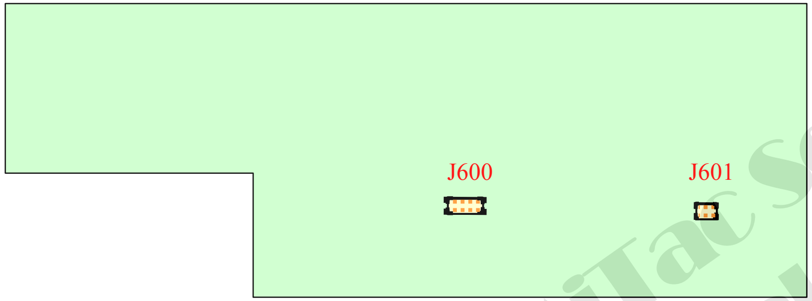
3.3 LED Board



- **HJ1: LED Board to MB Connector**

3. Definition & Location of Connectors/Switches

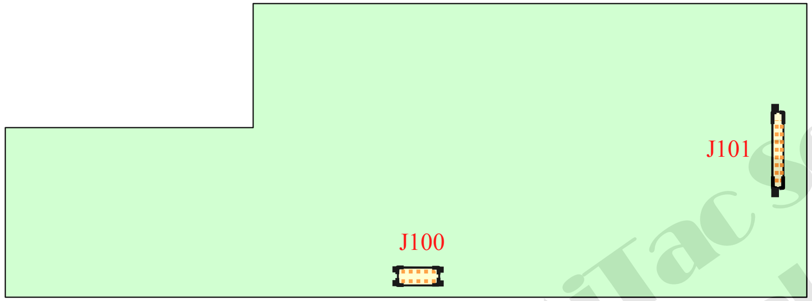
3.4 Touch Screen Board (Side A)



- **J600: Presume Pin Assignment**
- **J601: Touch Screen Cable Connector**

3. Definition & Location of Connectors/Switches

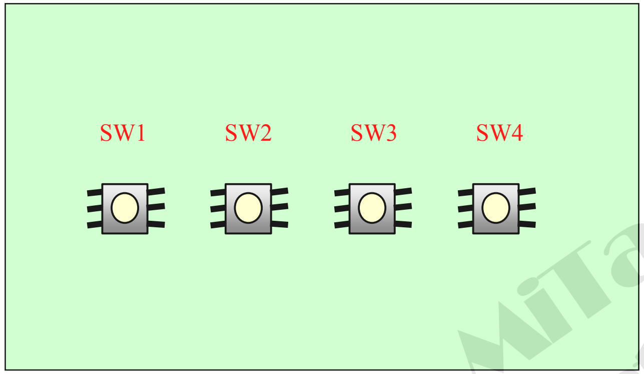
3.4 Touch Screen Board (Side B)



- **J100: Inverter Board to Touch Screen Board Connector**
- **J101: LCD Cable Connector**

3. Definition & Location of Connectors/Switches

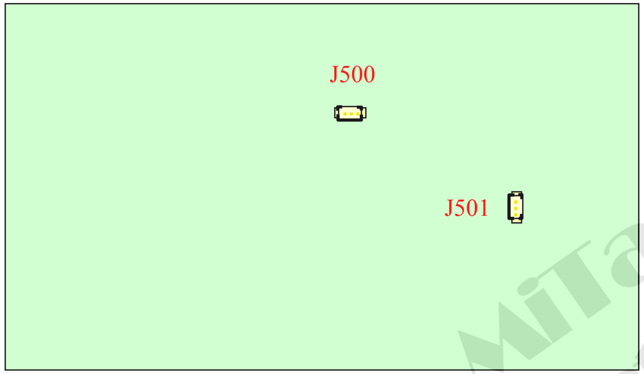
3.5 Switch Board (Side A)


SW1
SW2
SW3
SW4

- **SW1~SW4: Switch Button**

3. Definition & Location of Connectors/Switches

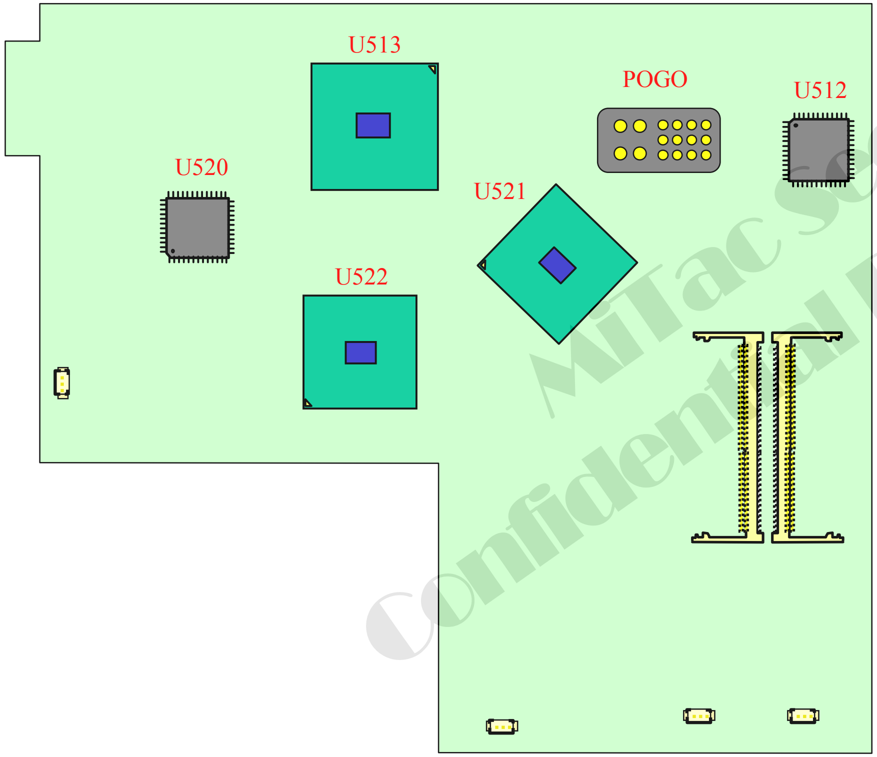
3.5 Switch Board (Side B)



- **J500: Touch Pad Connector**
- **J501: Switch Board to MB Connector**

4. Definition & Location of Major Components

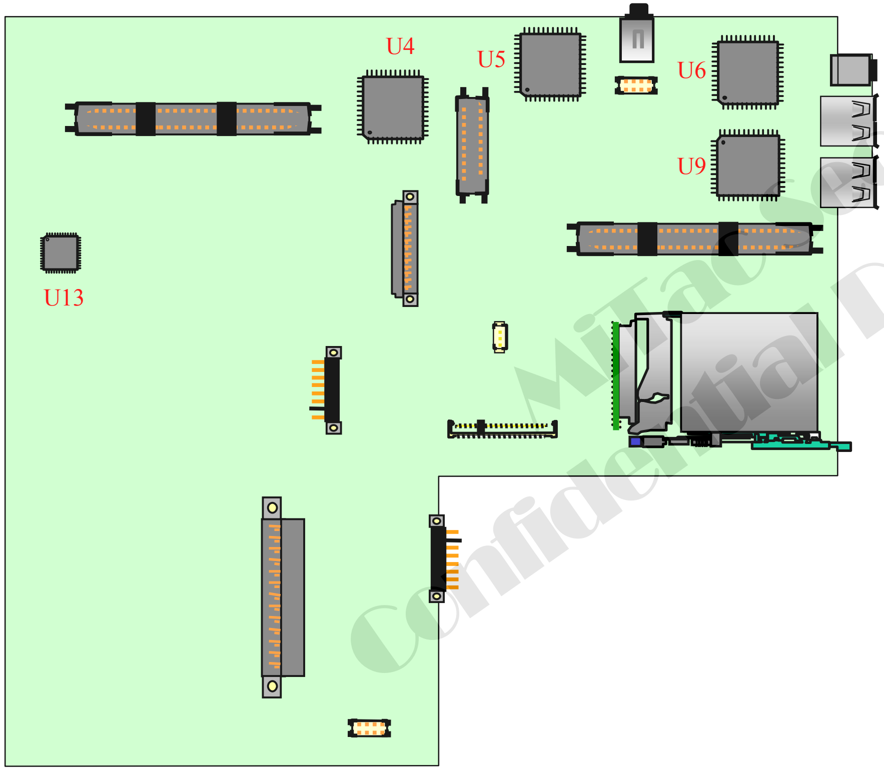
4.1 Mother Board (Side A)


U513
POGO
U512
U520
U521
U522

- **U512: System BIOS**
- **U513: Intel Yonah CPU Processor**
- **U520: PCMCIA & CardBus Controller**
- **U521: Intel 945GM North Bridge**
- **U522: Intel ICH7-M South Bridge**

4. Definition & Location of Major Components

4.1 Mother Board (Side B)



- **U4: Super I/O Controller**
- **U5: BCM5789M Giga LAN Controller**
- **U6: TI 1394B PHY**
- **U9: TI 1394B HOST**
- **U13: H8S/2140 Keyboard Controller**

5. Pin Descriptions of Major Components

5.1 Intel Yonah Processor CPU (1)

CPU Pin Description

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[31:3]#</td><td>I/O</td><td>A[31:]#(Address) define a 2*32- byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. Must connect the appropriate pins of both agents on the Intel Core TM Duo processor and the Intel Core TM Solo processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.</td></tr>
<tr><td>A20M#</td><td>I</td><td>If A20M#(Address-20 Mask) is asserted, the processor masks physical address bit 20(A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>I/O</td><td>ADS#(Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB#</td><td>I/O</td><td>Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr>
<tr><td>A[31:17]#</td><td>ADSTB[1]#</td></tr>
</table></td></tr>
<tr><td>BCLK[1:0]</td><td>I</td><td>The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.</td></tr>
<tr><td>BNR#</td><td>I/O</td><td>BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</td></tr>
</table>

CPU Pin Description (Continued)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BPM[2:1]#
BPM[3,0]#</td><td>I/O</td><td>BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.</td></tr>
<tr><td>BPRI#</td><td>I</td><td>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</td></tr>
<tr><td>BR0#</td><td>I/O</td><td>BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the Mobile Intel 945 Express chipset family (High Priority Agent).</td></tr>
<tr><td>BSEL[2:0]</td><td>O</td><td>BSEL[2:0] (Bus SELECT) are used to select the processor input clock frequency. The table defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The processor operates at 667 MHz or 533 MHz system bus frequency (166MHz or 133MHz BCLK[1:0] frequency, respectively).
BSE[2:0] Encoding for BCLK Frequency
<table>
<tr><th>BSEL[2]</th><th>BSEL[1]</th><th>BSE[0]</th><th>BCLK Frequency</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Reserved</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>133MHz</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Reserved</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>166MHz</td></tr>
</table></td></tr>
<tr><td>COMPP3:0]</td><td>Analog</td><td>COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.</td></tr>
</table>

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5.1 Intel Yonah Processor CPU (2)

CPU Pin Description (Continued)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN#/DSTBP#</th><th>DINV#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBR#</td><td>O</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.</td></tr>
</table>

CPU Pin Description (Continued)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DINV[3:0]#</td><td>I/O</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV[3]#</td><td>D[63:48]#</td></tr>
<tr><td>DINV[2]#</td><td>D[47:32]#</td></tr>
<tr><td>DINV[1]#</td><td>D[31:16]#</td></tr>
<tr><td>DINV[0]#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DPRSTP#</td><td>I</td><td>DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep Stated. In order to return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the Intel ICH7M chipset.</td></tr>
<tr><td>DPSLP#</td><td>I</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH7M chipset.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr>
</table></td></tr>
</table>

5.1 Intel Yonah Processor CPU (3)

CPU Pin Description (Continued)

Signal Name	Type	Description
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DINV[0]# / DSTBP[0]# D[31:16]#, DINV[1]# / DSTBP[1]# D[47:32]#, DINV[2]# / DSTBP[2]# D[63:48]#, DINV[3]# / DSTBP[3]#
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the Intel Architecture Software Developer's Manual and AP-485, For termination requirements please contact your Intel representative.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 VCCP . GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.Plese contact your Intel representative for more information regarding GTLREF implementation.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.

CPU Pin Description (Continued)

Signal Name	Type	Description
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	I	INIT#(Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers, The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write Instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction, INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Selt-Test(BIST).
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.

5.1 Intel Yonah Processor CPU (4)

CPU Pin Description (Continued)

Signal Name	Type	Description
LOCK#	I/O	When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	I/O	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. TCC will remain active until the system deasserts PRCCHOT#. By default PROCHOT# is configured as an output only. Bidirectional PROCHOT# must be enabled via the BIOS. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (HFM and LFM) and lower state (Deep Sleep and Deeper Sleep).
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
REQ[4:0]	I/O	REQ[4:0]#(Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications.

CPU Pin Description (Continued)

Signal Name	Type	Description
RESET#	I	On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. There is a 55 (normal) on die pull up resistor on this signal.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.

5.1 Intel Yonah Processor CPU (5)

CPU Pin Description (Continued)

Signal Name	Type	Description
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1,	I	TEST1 must have a stuffing option of separate pull down resistor to Vss.
TEST2	I	TEST2 must have a 51±5% pull down resistor to Vss.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
Vcc	I	Processor core power supply.
Vcca	I	Vcca provides isolated power for the internal processor core PLL's.
Vccp	I	Processor I/O Power Supply.
VID[6:0]	O	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. The VR must supply the voltage that is requested by the pins, or disable itself.

CPU Pin Description (Continued)

Signal Name	Type	Description
Vsssense	O	Vsssense together with Vccsense are voltage feedback signals to IMVP6 that control the 2.1m loadline at the processor die. It should be used to sense ground near the silicon with little noise.

5.2 Intel 945GM North Bridge (1)

Host Interface Signals

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** HBNR# is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-toinactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**CPU Reset:** The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH7 must provide processor frequency select strap setup and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the ICH7 driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** HDEFER# indicates that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.

Host Interface Signals (Continued)

Signal Name	Type	Description
HDRDY#	I/O GTL+	**Data Ready:** This signal is asserted for each cycle that data is transferred.
HEDRDY#	O GTL+	**Early Data Ready:** This signal indicates that the data phase of a read transaction will start on the bus exactly one common clock after assertion.
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** These signals are driven along with the HD[63:0] signals. They indicate if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8.. **HDINV[x]#** **Data Bits** HDINV3# HD[63:48] HDINV2# HD[47:32] HDINV1# HD[31:16] HDINV0# HD[15:0]
HA[31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, the HA[31:3]# are inputs. The (G)MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express* initiators. HA[31:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** These signals are the source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.
HD[63:0]#	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HHIT#	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. In addition, HHIT# is driven in conjunction with HHITM# by the target to extend the snoop window.

5.2 Intel 945GM North Bridge (2)

Host Interface Signals (Continued)

Signal Name	Type	Description
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** These signals are the differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence they are pseudo-differential, and not true differential. **Strobe** **Data** **Bits** HDSTBP3#, HDSTBN3# HD[63:48] HDINV3# HDSTBP2#, HDSTBN2# HD[47:32] HDINV2# HDSTBP1#, HDSTBN1# HD[31:16] HDINV1# HDSTBP0#, HDSTBN0# HD[15:00] HDINV0#
HHITM#	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. In addition, HHITM# is driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic (i.e., no DMI or PCI Express accesses to DRAM are allowed when HLOCK# is asserted by the processor).
HPCREQ#	I GTL+ 2X	**Precharge Request:** The processor provides a “hint” to the (G)MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The (G)MCH uses this information to schedule the read request to memory using the special “AutoPrecharge” attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. HPCREQ# is asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.
HREQ[4:0]#	I/O GTL+ 2X	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half, the signals carry additional information to define the complete transaction type.

Host Interface Signals (Continued)

Signal Name	Type	Description
HTRDY#	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Host Response Status:** These signals indicate the type of response as shown below: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by (G)MCH) 100 = Hard Failure (not driven by (G)MCH) 101 = No data response 110 = Implicit Write back 111 = Normal data response
BSEL[2:0]	I COMS	**Bus Speed Select:** At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.
HRCOMP	I/O COMS	**Host RCOMP:** This signal is used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V_{TT}).
HSCOMP	I/O COMS	**Slew Rate Compensation:** This is the compensation signal for the Host Interface.
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HDVREF	I A	**Host Reference Voltage:** Voltage input for the data, address, and common clock signals of the Host GTL interface.
HACCVREF	I A	**Host Reference Voltage:** Reference voltage input for the Address, and Common clock signals of the Host GTL interface.

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (VTT).

5.2 Intel 945GM North Bridge (3)

DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Ax and its complement SCLK_Ax# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_A[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_A[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_A#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-1.8 2X	**Data Lines:** The SDQ_A[63:0] signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax bit for every data byte lane.
SDQS_A[7:0]	I/O SSTL-1.8 2X	**Data Strobes:** For DDR2, SDQS_Ax and its complement SDQS_Ax# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.

DDR2 DRAM Channel A Interface (Continued)

Signal Name	Type	Description
SDQS_A[7:0]#	I/O SSTL-1.8 2X	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Ax is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Bx and its complement SCLK_Bx# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary Differential DDR2 Clock signals.
SCS_B[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank). These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_B[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_B[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology is 8 banks.
SRAS_B#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.

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DDR2 DRAM Channel B Interface (Continued)

Signal Name	Type	Description
SCAS_B#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-1.8 2X	**Data Lines:** The SDQ_B[63:0] signals interface to the SDRAM data bus.
SDM_B[7:0]	O SSTL-1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx bit for every data byte lane.
SDQS_B[7:0]	I/O SSTL-1.8 2X	**Data Strobes:** For DDR2, SDQS_Bx and its complement SDQS_Bx# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[7:0]#	I/O SSTL-1.8 2X	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_B[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Bx is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

PCI Express* Interface Signals

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I/O PCIE	**PCI Express* Receive Differential Pair**
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	**PCI Express* Transmit Differential Pair**
EXP_ICOMPO	I A	**PCI Express* Output Current and Resistance Compensation**
EXP_COMPI	I A	**PCI Express* Input Current Compensation**

Unless otherwise specified, PCI Express signals are AC coupled, so the only voltage specified is a maximum 1.2 V differential swing.

Analog Display Signals (Intel® 82945G GMCH Only)

Signal Name	Type	Description
RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
RED#	O A	**REDB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance: however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 ΩCRT load).
GREEN#	O A	**GREENB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
BLUE#	O A	**BLUEB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
REFSET	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 Ω 1% resistor is required between REFSET and motherboard ground.
HSYNC	O 2.5V CMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”. 2.5 V output.
VSYNC	O 2.5V CMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). 2.5 V output.
DDC_CLK	I/O 2.5V CMOS	**Monitor Control Clock:** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
DDC_DATA	I/O 2.5V CMOS	**Monitor Control Data:** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

5.2 Intel 945GM North Bridge (5)

Clock, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I HCSL	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Memory domain clocks are also derived from this source.
GCLKP GCLKN	I HCSL	**Differential PCI Express* Clock In:** These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I HCSL	**Display PLL Differential Clock In**
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH7. All PCI Express graphics attach output signals will also tri-state compliant to *PCI Express* Specification, Revision 1.0a*. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
EXTTS#	I CMOS	**External Thermal Sensor Input:** This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.
EXP_EN	I CMOS	**PCI Express SDVO Concurrent Select:** 0 = Only SDVO or PCI Express operational 1 = SDVO and PCI Express operating simultaneously via PCI Express port **NOTES:** For the 82945P MCH, this signal should be pulled low.
EXP_SLR	I CMOS	**PCI Express* Lane Reversal/Form Factor Selection:** (G)MCH's PCI Express lane numbers are reversed to differentiate Balanced Technology Extended (BTX) or ATX form factors. 0 = (G)MCH's PCI Express lane numbers are reversed (BTX Platforms) 1 = Normal operation (ATX Platforms)
ICH_SYNC#	O HVCMOS	**ICH Sync:** This signal is connected to the MCH_SYNCH# signal on the ICH7.

Clock, Reset, and Miscellaneous (Continued)

Signal Name	Type	Description
XORTEST	I/O GTL+	**XOR Test:** This signal is used for Bed of Nails testing by OEMs to execute XOR Chain test.
LLLZTEST	I/O GTL+	**All Z Test:** As an input this signal is used for Bed of Nails testing by OEMs to execute XOR Chain test. It is used as an output for XOR chain testing.

DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[1:0]	I/O	**System Memory RCOMP**
SOCOMP[1:0]	I/O A	**DDR2 On-Die DRAM Over Current Detection (OCD) Driver Compensation**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** These signals are reference voltage inputs for each SDQ_x, SDM_x, SDQS_x, and SDQS_x# input signals.

Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I/O DMI	**Direct Media Interface:** These signals are receive differential pairs (Rx).
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** These signals are transmit differential pairs (Tx).

5.2 Intel 945GM North Bridge (6)

Intel® Serial DVO (SDVO) Interface (Intel® 82945G GMCH Only)

Signal Name	Type	Description
SDVOB_CLK-	O PCIE	**Serial Digital Video Channel B Clock Complement:** This signal is multiplexed with EXP_TXN12.
SDVOB_CLK+	O PCIE	**Serial Digital Video Channel B Clock Clock:** This signal is multiplexed with EXP_TXP12.
SDVOB_RED-	O PCIE	**Serial Digital Video Channel C Red Complement:** This signal is multiplexed with EXP_TXN15.
SDVOB_RED+	O PCIE	**Serial Digital Video Channel C Red:** This signal is multiplexed with EXP_TXP15.
SDVOB_GREEN-	O PCIE	**Serial Digital Video Channel B Green Complement:** This signal is multiplexed with EXP_TXN14.
SDVOB_GREEN+	O PCIE	**Serial Digital Video Channel B Green:** This signal is multiplexed with EXP_TXP14.
SDVOB_BLUE-	O PCIE	**Serial Digital Video Channel B Blue Complement:** This signal is multiplexed with EXP_TXN13.
SDVOB_BLUE+	O PCIE	**Serial Digital Video Channel B Blue:** This signal is multiplexed with EXP_TXP13.
SDVOC_RED-/ SDVOB_ALPHA-	O PCIE	**Serial Digital Video Channel C Red Complement Channel B Alpha Complement:** This signal is multiplexed with EXP_TXN11.
SDVOC_RED+/ SDVOB_ALPHA+	O PCIE	**Serial Digital Video Channel C Red Complement Channel B Alpha:** This signal is multiplexed with EXP_TXP11.
SDVOC_GREEN-	O PCIE	**Serial Digital Video Channel C Green Complement:** This signal is multiplexed with EXP_TXN10.
SDVOC_GREEN+	O PCIE	**Serial Digital Video Channel C Green:** This signal is multiplexed with EXP_TXP10.
SDVOC_BLUE-	O PCIE	**Serial Digital Video Channel C Blue Complement:** This signal is multiplexed with EXP_TXN9.
SDVOC_BLUE+	O PCIE	**Serial Digital Video Channel C Blue:** This signal is multiplexed with EXP_TXP9.
SDVOC_CLK-	O PCIE	**Serial Digital Video Channel C Clock Complement:** This signal is multiplexed with EXP_TXN8.
SDVOC_CLK+	O PCIE	**Serial Digital Video Channel C Clock:** This signal is multiplexed with EXP_TXP8.
SDVO_TVCLKIN-	I PCIE	**Serial Digital Video TV-OUT Synchronization Clock Complement:** This signal is multiplexed with EXP_RXN15.
SDVO_TVCLKIN+	I PCIE	**Serial Digital Video TV-OUT Synchronization Clock:** This signal is multiplexed with EXP_RXP15.
SDVOB_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement:** This signal is multiplexed with EXP_RXN14.

Intel® Serial DVO (SDVO) Interface (Intel® 82945G GMCH Only) (Continued)

Signal Name	Voltage	Description
SDVOB_INT+	I PCIE	**Serial Digital Video Input Interrupt:** This signal is multiplexed with EXP_RXP14.
SDVOC_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement:** This signal is multiplexed with EXP_RXN10.
SDVOC_INT+	I PCIE	**Serial Digital Video Input Interrupt:** This signal is multiplexed with EXP_RXP10.
SDVO_STALL-	I PCIE	**Serial Digital Video Filed Stall Complement:** This signal is multiplexed with EXP_RXN13.
SDVO_STALL+	I PCIE	**Serial Digital Video Filed Stall:** This signal is multiplexed with EXP_RXP13.
SDVO_CTRLCLK	I/O COD	**Serial Digital Video Device Control Clock.**
SDVO_CTRLDATA	I/O COD	**Serial Digital Video Device Control Data.**

Power and Ground

Name	Voltage	Description
VCC	1.5V	Core Power
VTT	1.2V	Processor System Bus Power
VCC_EXP	1.5V	PCI Express* and DMI Power
VCCSM	1.8V	System Memory Power
VCC2	2.5V	2.5V COMS Power
VCCA_EXPPLL	1.5V	PCI Express PLL Analog Power
VCCA_DPLLA (GMCH ONLY)	1.5V	Display PLL A Analog Power
VCCA_DPLLB (GMCH ONLY)	1.5V	Display PLL B Analog Power
VCCA_HPLL	1.5V	Host PLL Analog Power
VCCA_SMPLL	1.5V	System Memory PLL Analog Power
VCCA_DAC	2.5V	Display DAC Analog Power
VSS	0V	Ground
VSSA_DAC	0V	Ground

5.3 Intel ICH7-M South Bridge (1)

PCI Interface Signals

Signal Name	Type	Description
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH7's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH7 has valid data present on AD[31:0]. During a read, it indicates the ICH7 is prepared to latch data. IRDY# is an input to the ICH7 when the ICH7 is the target and an output from the ICH7 when the ICH7 is an initiator. IRDY# remains tri-stated by the ICH7 until driven by an initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the Intel® ICH7's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH7, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH7, as a target is prepared to latch data. TRDY# is an input to the ICH7 when the ICH7 is the initiator and an output from the ICH7 when the ICH7 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH7 until driven by a target.
STOP#	I/O	**Stop:** STOP# indicates that the ICH7, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH7, as an initiator, to stop the current transaction. STOP# is an output when the ICH7 is a target and an input when the ICH7 is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH7 counts the number of one within the 36 bits plus PAR and the sum is always even. The ICH7 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH7 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH7 drives and tristates PAR identically to the AD[31:0] lines except that the ICH7 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH7 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH7 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH7 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH7 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel® ICH7 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]#** **Command Type** 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH7 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH7 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH7 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH7 address or an address destined DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH7-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH7 until driven by a target device.
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH7 when the ICH7 is the target, and FRAME# is an output from the ICH7 when the ICH7 is the initiator. FRAME# remains tristated by the ICH7 until driven by an initiator.

5.3 Intel ICH7-M South Bridge (2)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH7 drives PERR# when it detects a parity error. The ICH7 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[0:3]# **REQ[4]#/** GPIO22 **REQ[5]#**/GPIO1	I	**PCI Requests:** The ICH7 supports up to 6 masters on the PCI bus. The REQ[4]# and REQ5# pins can instead be used as a GPIO.
GNT[0:3]# **GNT[4]#/** GPIO48 **GNT[5]#/** GPIO17#	O	**PCI Grants:** The ICH7 supports up to 6 masters on the PCI bus. The GNT4# and GNT5# pins can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT5#/GPIO17 has an internal pull-up.
PCICLK	I	**NOTE: PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus.
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. The ICH7 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus in desktop configurations.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH7 has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH7 may drive PME# active due to an internal wake event. The ICH7 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

Serial ATA Interface Signals

Name	Type	Description
SATA0TXP **SATA0TXN**	O	**Serial ATA 0 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 0.
SATA0RXP **SATA0RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0.
SATA1TXP **SATA1TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1.
SATA1RXP **SATA1RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1.
SATA2TXP **SATA2TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2.
SATA2RXP **SATA2RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2.
SATA3TXP **SATA3TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3.
SATA3RXP **SATA3RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3.
SATARBIAS	O	**Serial ATA Resistor Bias:** These are analog connection points for an external resistor to ground.
SATARBIAS#	I	**Serial ATA Resistor Bias Complement:** These are analog connection points for an external resistor to ground.
SATA0GP/ **GPIO21**	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to ‘0’ to indicate that the switch is closed and to ‘1’ to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP/ **GPIO19**	I	**Serial ATA 1 General Purpose:** Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP/ **GPIO36**	I	**Serial ATA 2 General Purpose:** Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36.

5.3 Intel ICH7-M South Bridge (3)

Serial ATA Interface Signals (Continued)

Name	Type	Description
SATA3GP/ GPIO37	I	**Serial ATA 3 General Purpose:** Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37.
SATALED#	OC	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. **NOTE:** An internal pull-up is enabled only during PLTRST# assertion.
SATACLKREQ #/GPIO35	OD (Native)/ I/O (GP)	**Serial ATA Clock Request:** This is an open-drain output pin when configured as SATACLKREQ#. It is to connect to the system clock chip. When active, request for SATA Clock running is asserted. When tri-stated, it tells the Clock Chip that SATA Clock can be stopped. An external pull-up resistor is required.

Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS#	I/O	**SPI Chip Select:** Also used as the SPI bus request signal.
SPI_MISO	I	**SPI Master IN Slave OUT:** Data input pin for Intel® ICH7.
SPI_MOSI	O	**SPI Master OUT Slave IN:** Data output pin for ICH7.
SPI _ARB	I	**SPI Arbitration:** SPI arbitration signal is used to arbitrate the SPI bus with Intel PRO 82573E Gigabit Ethernet Controller when Shared Flash is implemented.
SPI_CLK	O	**SPI Clock:** SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz.

Platform LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** This signal is driven by the Platform LAN Connect component. The frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The Platform LAN Connect component uses these signals to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data:** The integrated LAN controller uses these signals to transfer data and control information to the Platform LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The Platform LAN Connect component’s Reset and Sync signals are multiplexed onto this pin.

Other Clock

Name	Type	Description
CLK14	I	**Oscillator Clock:** This clock is used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. Runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the SATA controller at 100 MHz. This clock is permitted to stop during S3/S4/S5 states.
DMI_CLKP, DMI_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the Direct Media Interface. Runs at 100 MHz.

5.3 Intel ICH7-M South Bridge (4)

IDE Interface Signals

Name	Type	Description
DCS1#	O	**IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the IDE connector.
DCS3#	O	**IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the IDE connector.
DA[2:0]	O	**IDE Device Address:** These output signals are connected to the corresponding signals on the IDE connector. They are used to indicate which byte in either the ATA command block or control block is being addressed.
DD[15:0]	I/O	**IDE Device Data:** These signals directly drive the corresponding signals on the IDE connector. There is a weak internal pull-down resistor on DD7.
DDREQ	I	**IDE Device DMA Request:** This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pulldown resistor on this signal.
DDACK#	O	**IDE Device DMA Acknowledge:** This signal directly drives the DAK# signal on the IDE connector. DDACK# is asserted by the Intel® ICH7 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
DIOR#/ (DWSTB/ RDMARDY#)	O	**DIOR# /Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the DD lines. Data is latched by the ICH7 on the deassertion edge of DIOR#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH7 drives valid data on rising and falling edges of DWSTB. Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH7 deasserts RDMARDY# to pause burst data transfers.

IDE Interface Signals (Continued)

Name	Type	Description
DIOW#/ (DSTOP)	O	**Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the DD lines. Data is latched by the IDE device on the deassertion edge of DIOW#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Stop (Ultra DMA): ICH7 asserts this signal to terminate a burst.
IORDY/ (DRSTB/ WDMARDY#)	I	**I/O Channel Ready (PIO):** This signal will keep the strobe active (DIOR# on reads, DIOW# on writes) longer than the minimum width. It adds wait-states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, ICH7 latches data on rising and falling edges of this signal from the disk. Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is deasserted by the disk to pause burst data transfers.

System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPIO if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT#	I/OD	**SMLink Alert:** Output of the integrated LAN and input to either the integrated ASF or an external management controller in order for the LAN's SMLINK slave to be serviced.

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USB Interface Signals

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port [1:0] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The Intel® ICH7 integrates 15 k Ω pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port [3:2] Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH7 integrates 15 K Ω ?pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	**Universal Serial Bus Port [5:4] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH7 integrates 15 K Ω ?pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP6P, USBP6N, USBP7P, USBP7N	I/O	**Universal Serial Bus Port [7:6] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH7 integrates 15 K Ω ?pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
OC[4:0]# OC5#/GPIO29 **OC6#**/GPIO30 **OC7#**/GPIO31	I	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:4]# may optionally be used as GPIOs. **NOTE:** OC[7:0]# are not 5 V tolerant.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock:** Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In:** Transfers data from the EEPROM to the Intel® ICH7. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out:** Transfers data from the ICH7 to the EEPROM.
EE_CS	O	**EEPROM Chip Select:** Chip select signal to the EEPROM.

Interrupt Signals

Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the *Interrupt Steering* section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IDEIRQ	I	**IDE Interrupt Request:** This interrupt input is connected to the IDE drive.

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Power Management Interface Signals

Name	Type	Description
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pullup resistor and has an internal 16 ms de-bounce on the input.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH7 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller will be put into reset. This signal must be asserted for at least 10 ms after the resume well power (VccSus3_3 and VccSus1_5) is valid. When de-asserted, this signal is an indication that the resume well power is stable. **NOTE:** LAN_RST# should be tied to RSMEST#.
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wakeup.
MCH_SYNC#	I	**MCH SYNC:** This input is internally ANDed with the PWROK input. Connected to the ICH_SYNC# output of (G)MCH.
THRM#	I	**Thermal Alarm:** Active low signal generated by external hardware to generate an SMI# or SCI.
THRMTRIP#	I	**Thermal Trip:** When low, this signal indicates that a thermal trip from the processor occurred, and the ICH7 will immediately transition to a S5 state. The ICH7 will not wait for the processor stop grant cycle since the processor has overheated.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH7 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.

Power Management Interface Signals (Continued)

Name	Type	Description
SUSCLK	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.
VRMPWRGD	I	**VRM Power Good:** This should be connected to be the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input.
PLTRST#	O	**Platform Reset:** The Intel® ICH7 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, IDE, TPM, etc.). The ICH7 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH7 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH7 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the VccSus3_3 well.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power to use the ICH7's DRAM power-cycling feature. Refer to Chapter 5.14.10.2 for details.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH7 that core power has been stable for 99 ms and that PCICLK has been stable for 1 ms. An exception to this rule is if the system is in S3HOT, in which PWROK may or may not stay asserted even though PCICLK may be inactive. PWROK can be driven asynchronously. When PWROK is negated, the ICH7 asserts PLTRST#. **NOTE:** PWROK must deassert for a minimum of three RTC clock periods for the ICH7 to fully reset the power and properly generate the PLTRST# output.

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Processor Interface Signals

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The Intel® ICH7 can optionally assert the CPUSLP# signal when going to the S1 state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH7 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is asserted, the ICH7 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH7 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor. Error register is written, the IGNNE# signal is not asserted.
INIT#	O	**Initialization:** INIT# is asserted by the ICH7 for 16 PCI clocks to reset the processor. ICH7 can be configured to support processor Built In Self Test (BIST).
INIT3_3V#	O	**Initialization 3.3 V:** This is the identical 3.3 V copy of INIT# intended for Firmware Hub.
INTR	O	**Processor Interrupt:** INTR is asserted by the ICH7 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH7 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH7 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH7 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH7's other sources of INIT#. When the ICH7 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH7 will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD/ GPIO49	O	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input to indicate when the CPU power is valid. This is an output signal that represents a logical AND of the ICH7's PWROK and VRMPWRGD signals. This signal may optionally be configured as a GPIO.

Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals:** These signals are multiplexed with the LPC address signals.
FWH4/ LFRAME#	O	**Firmware Hub Signals:** This signal is multiplexed with the LPC LFRAME# signal.

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General Purpose I/O Signals

Name	Type	Tolerance	Power Well	Description
GPIO49	I/O	V_CPU_IO	V_CPU_IO	Multiplexed with CPUPWRGD
GPIO48	I/O	3.3 V	Core	Multiplexed with GNT4#
GPIO[47:40]	N/A	3.3 V	N/A	Not implemented.
GPIO[39:38]	I/O	3.3 V	Core	Unmultiplexed.
GPIO37	I/O	3.3 V	Core	Multiplexed with SATA3GP.
GPIO36	I/O	3.3 V	Core	Multiplexed with SATA2GP.
GPIO35	I/O	3.3 V	Core	Multiplexed with SATACLKREQ#.
GPIO34	I/O	3.3 V	Core	Unmultiplexed.
GPIO33	I/O	3.3 V	Core	Unmultiplexed.
GPIO32	I/O	3.3 V	Core	Unmultiplexed.
GPIO31	I/O	3.3 V	Resume	Multiplexed with OC7#
GPIO30	I/O	3.3 V	Resume	Multiplexed with OC6#
GPIO29	I/O	3.3 V	Resume	Multiplexed with OC5#
GPIO28	I/O	3.3 V	Resume	Unmultiplexed.
GPIO27	I/O	3.3 V	Resume	Unmultiplexed.
GPIO26	I/O	3.3 V	Resume	Unmultiplexed.
GPIO25	I/O	3.3 V	Resume	Unmultiplexed.
GPIO24	I/O	3.3 V	Resume	Unmultiplexed. Not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Multiplexed with LDRQ1#
GPIO22	I/O	3.3 V	Core	Multiplexed with REQ4#
GPIO21	I/O	3.3 V	Core	Multiplexed with SATA0GP.
GPIO20	I/O	3.3 V	Core	Unmultiplexed.
GPIO19	I/O	3.3 V	Core	Multiplexed with SATA1GP.
GPIO18	I/O	3.3 V	Core	Unmultiplexed.
GPIO17	I/O	3.3 V	Core	Multiplexed with GNT5#.
GPIO16	I/O	3.3 V	Core	Unmultiplexed.
GPIO[15:12]	I/O	3.3 V	Resume	Unmultiplexed.
GPIO11	I/O	3.3 V	Resume	Multiplexed with SMBALERT#
GPIO[10:8]	I/O	3.3 V	Resume	Unmultiplexed.
GPIO[7:6]	I/O	3.3 V	Core	Unmultiplexed.
GPIO[5:2]	I/OD	5 V	Core	Multiplexed with PIRQ[H:E]#.

General Purpose I/O Signals (Continued)

Name	Type	Tolerance	Power Well	Description
GPIO1	I/O	5 V	Core	Multiplexed with REQ5#.
GPIO0	I/O	3.3 V	Core	Unmultiplexed.

NOTES:

1. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.
2. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some ICH7 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH7 driving a pin to a logic 1 to another device that is powered down..

PCI Express* Signals

Name	Type	Description
PETp[1:4], PETn[1:4]	O	**PCI Express* Differential Transmit Pair 1:4**
PERp[1:4], PERn[1:4]	I	**PCI Express Differential Receive Pair 1:4**
PETp[5:6], PETn[5:6] (Intel® ICH7R Only)	O	**PCI Express* Differential Transmit Pair 5:6** **Reserved: ICH7**
PERp[1:4], PERn[5:6] (ICH7R Only)	I	**PCI Express Differential Receive Pair 5:6** **Reserved: ICH7**

SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up resistor is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up resistor is required.
SMBALERT#/ GPIO11	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPIO.

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AC’97/Intel® High Definition Auto Link Signals

Name	Type	Description
ACZ_RST#	O	**AC’97/Intel® High Definition Audio Reset:** Master hardware reset to external codec(s).
ACZ_SYNC	O	**AC ’97/Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number.
ACZ_BIT_CLK	I/O	**AC ’97 Bit Clock Input:** 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor (see Note below). **Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the Intel® ICH7). This signal has an integrated pull-down resistor so that ACZ_BIT_CLK doesn’t float when an Intel High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC ’97.
ACZ_SDOUT	O	**AC ’97/Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. **NOTE:** ACZ_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Function Straps for more details. There is a weak integrated pull-down resistor on the ACZ_SDOUT pin.
ACZ_SDIN[2:0]	I	**AC ’97/Intel High Definition Audio Serial Data In [2:0]:** Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio. These signals have integrated pulldown resistors, which are always enabled.

LPC Interface Signals

Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME#/ FWH4	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[0]# **LDRQ[1]#**/ GPIO23	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

Power and Ground Signals

Name	Description
Vcc3_3	3.3 V supply for core well I/O buffers (22 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_05	1.05 V supply for core well logic (20 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for Logic and I/O (30 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for Logic and I/O (53 pins). This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs (2 pins). This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3.3 V supply for resume well I/O buffers (24 pins). This power is not expected to be shut off unless the system is unplugged in desktop configurations.
VccSus1_05	1.05 V supply for resume well logic (5 pins). This power is not expected to be shut off unless the system is unplugged in desktop configurations. This voltage may be generated internally (see Function Straps for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF_Sus	Reference for 5 V tolerance on resume well inputs (1 pin). This power is not expected to be shut off unless the system is unplugged in desktop configurations.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well (1 pin). This power is not expected to be shut off unless the RTC battery is removed or completely drained. **Note:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Intel® ICH7-based platform can be done by using a jumper on RTCRST# or GPI.
VccUSBPLL	1.5 V supply for core well logic (1 pin). This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if USB not used.
VccDMIPLL	1.5 V supply for core well logic (1 pins. This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.
VccSATAPLL	1.5 V supply for core well logic (1 pins). This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if SATA not used.
V_CPU_IO	Powered by the same supply as the processor I/O voltage (3 pins). This supply is used to drive the processor interface signals listed in Process Interface Signals.
Vss	Grounds (194 pins).

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Functional Strap Definitions

Signal	Usage	When Sampled	Description
GNT3#	Top-Block Swap Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (Intel® ICH7 inverts A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT2#	Reserved		This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
REQ[4:1]#	XOR Chain Selection	Rising Edge of PWROK	See Chapter 25 for functionality information.
LINKALERT#	Reserved		This signal requires an external pull-up resistor.
SPKR	No Reboot	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (ICH7 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
INTVRMEN	Integrated VccSus1_05 VRM Enable/ Disable	Always	Enables integrated VccSus1_05 VRM when sampled high.
EE_CS	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
EE_DOUT	Reserved		This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection	Rising Edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups.Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11:10) (GNT5# is MSB) 01-SPI 10-PCI 11-LPC

Functional Strap Definitions (Continued)

Signal	Usage	When Sampled	Description
ACZ_SDOUT	XOR Chain Entrance/PCI Express* Port Config bit 1	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. See Chapter 25 for XOR Chain functionality information. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 7.1.34 for details. This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Port Config bit 0	Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers:Offset 224h). See Section 7.1.34 for details.
GPIO25	Reserved	Rising Edge of RSMRST#	This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
GPIO16	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
SATALED#	Reserved		This signal has a weak internal pull-up enabled only when PLTRST# is asserted. **NOTE:** This signal should not be pulled low.
TP3	XOR Chain Entrance	Rising Edge of PWROK	See Chapter 25 for functionality information. This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low unless using XOR Chain testing.

Direct Media Interface Signals

Name	Type	Description
DMI[0:3]TXP, DMI[0:3]TXN	O	**Direct Media Interface Differential Transmit Pair 0:3**
DMI[0:3]RXP, DMI[0:3]RXN	I	**Direct Media Interface Differential Receive Pair 0:3**
DMI_ZCOMP	O	**Impedance Compensation Input:** Determines DMI input impedance.
DMI_IRCOMP	I	**Impedance/Compensation Compensation Output:** Determines DMI output impedance and bias current.

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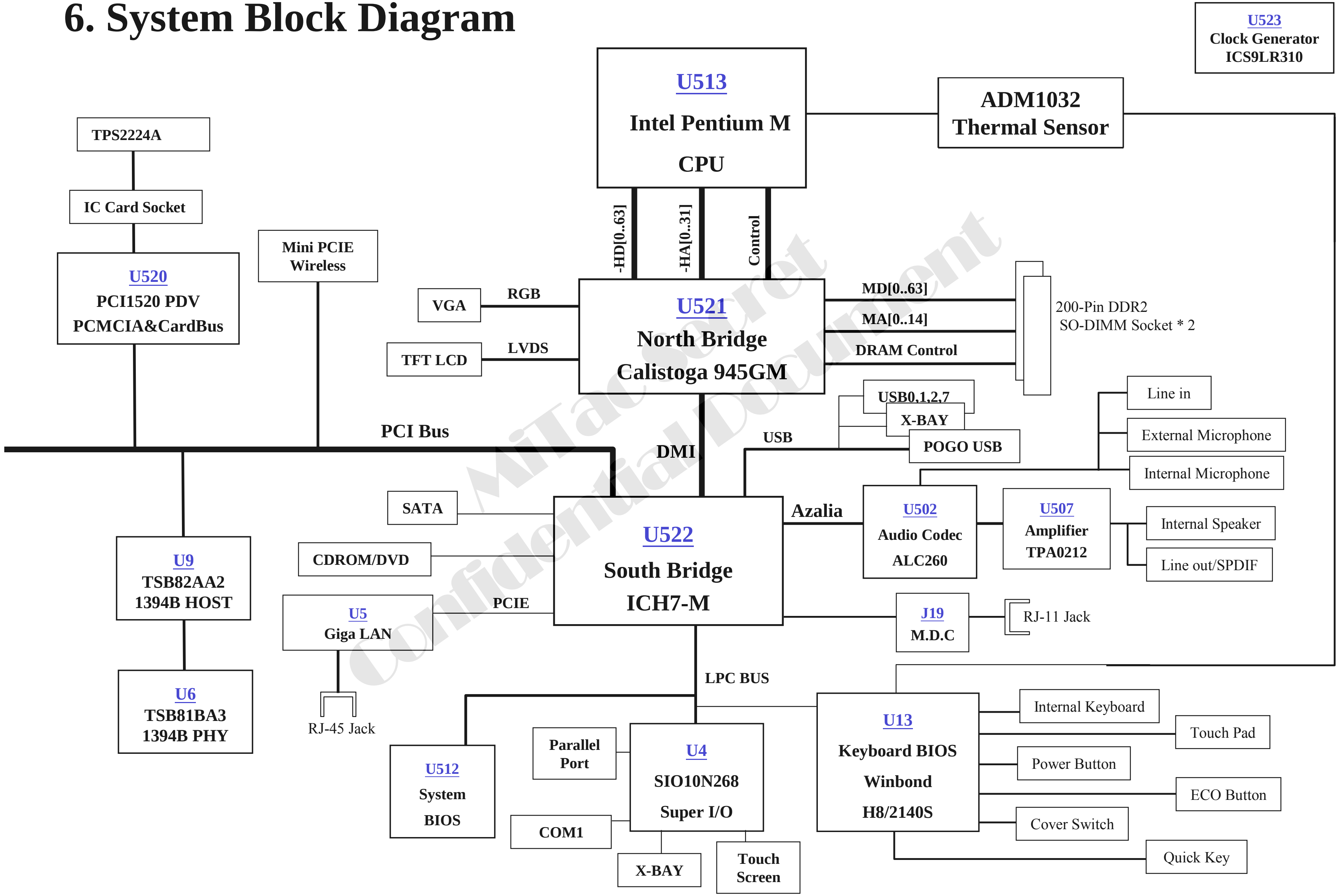
Miscellaneous Signals

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal 1.05 V Suspend regulator when connected to VccRTC. When connected to Vss, the internal regulator is disabled.
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap. See Function Straps for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. **NOTES:** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
TP0	I	**Test Point 0:** This signal must have an external pull-up to VccSus3_3.
TP1	O	**Test Point 1:** Route signal to a test point.
TP2	O	**Test Point 2:** Route signal to a test point.
TP3	I/O	**Test Point 3:** Route signal to a test point.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX2 should be left floating.

6. System Block Diagram


U523
Clock Generator
ICS9LR310
U513
Intel Pentium M
CPU
ADM1032
Thermal Sensor
TPS2224A
IC Card Socket
U520
PCI1520 PDV
PCMCIA&CardBus
Mini PCIE
Wireless
-HD[0..63]
-HA[0..31]
Control
VGA
RGB
TFT LCD
LVDS
U521
North Bridge
Calistoga 945GM
MD[0..63]
MA[0..14]
DRAM Control
200-Pin DDR2
SO-DIMM Socket * 2
USB0,1,2,7
X-BAY
POGO USB
USB
PCI Bus
DMI
Line in
External Microphone
Internal Microphone
SATA
CDROM/DVD
U522
South Bridge
ICH7-M
Azalia
U502
Audio Codec
ALC260
U507
Amplifier
TPA0212
Internal Speaker
Line out/SPDIF
U9
TSB82AA2
1394B HOST
U5
Giga LAN
PCIE
J19
M.D.C
RJ-11 Jack
RJ-45 Jack
LPC BUS
U6
TSB81BA3
1394B PHY
U512
System
BIOS
Parallel
Port
U4
SIO10N268
Super I/O
COM1
X-BAY
Touch
Screen
U13
Keyboard BIOS
Winbond
H8/2140S
Internal Keyboard
Touch Pad
Power Button
ECO Button
Cover Switch
Quick Key

7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This Power on Self Test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the debug card plug at Parallel port.

7.2 Maintenance Diagnostics

7.2.1 Diagnostic Tool for Mini PCI Slot

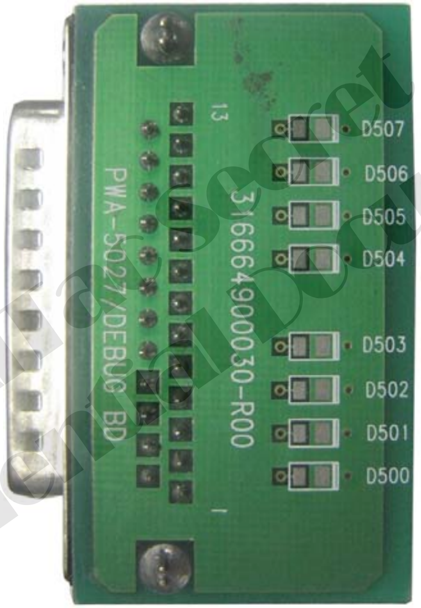

13
316664900030-R00
PWA-5027/DEBUG BD
D507
D506
D505
D504
D503
D502
D501
D500
1

Figure 7-1 Mini PCI debug card
P/N: 316664900030-R00
Description: PWA-5027/DEBUG BD

7.3 Error Codes-1

Following is a list of error codes in sequent display on the Mini PCI debug board.

Tpoint	Post Routine Description
02h	Verify Real Mode. If the CPU is in protected mode, turn on A20 and pulse the reset line, forcing a shutdown 0. NOTE: Hook routine should not alter DX, which holds the powerup CPU ID.
03h	Disable Non-Maskable Interrupts.
04h	Get CPU type from CPU registers and other methods. Save CPU type in NVRAM. NOTE: Hook routine should not alter DX, which holds the powerup CPU ID.
06h	Initialize system hardware. Reset the DMA controllers, disable the videos, clear any pending interrupts from the real-time clock and set up port B register.
07h	Disable system ROM shadow and start to execute ROMEXEC code from the flash part. This task is pulled into the build only when the ROMEXEC relocation is installed.
08h	Initialize chip set registers to the Initial POST Values.
09h	Set in-POST flag in CMOS that indicates we are in POST. If this bit is not cleared by postClearBootFlagJ (AEh), the TrustedCore on next boot determines that the current configuration caused POST to fail and uses default values for configuration. Clear the
0ah	Initialize CPU registers
0bh	Enable CPU cache. Set bits in cmos related to cache.
0ch	Set the initial POST values of the cache registers if not integrated into the chipset.
0eh	Set the initial POST values for registers in the integrated I/O chip.
0fh	Enable the local bus IDE as primary or secondary depending on other drives detected.
10h	Initialize Power Management.
11h	General dispatcher for alternate register initialization. Set initial POST values for other hardware devices defined in the register tables.
12h	Restore the contents of the CPU control word whenever the CPU is reset.
13h	Early reset of PCI devices required to disable bus master. Assumes the presence of a stack and running from decompressed shadow memory.
14h	Verify that the 8742 keyboard controller is responding. Send a self-test command to the 8742 and wait for results. Also read the switch inputs from the 8742 and write the keyboard controller command byte.
16h	Verify that the ROM BIOS checksums to zero
17h	Initialize external cache before autosizing memory.

7.3 Error Codes-2

Tpoint	Post Routine Description
18h	Initialize all three of the 8254 timers. Set the clock timer (0) to binary count, mode 3 (square wave mode), and read/write LSB then MSB. Initialize the clock timer to zero. Set the RAM refresh timer (1) to binary count, mode 2 (Rate Generator), and read/
1ah	Initialize DMA command register with these settings:
	1. Memory to memory disabled 2. Channel 0 hold address disabled 3. Controller enabled 4. Normal timing 5. Fixed priority 6. Late write selection 7. DREQ sense active 8. DACK sense active low.Initialize all 8 DMA channels with these settings: 1. Single mode 2. Address increment 3. Auto initialization disabled (channel 4 - Cascade) 4,. Verify transfer
1ch	Initialize interrupt controllers for some shutdowns.
20h	Verify that DRAM refresh is operating by polling the refresh bit in PORTB.
22h	Reset the keyboard.
24h	Set segment-register addressibility to 4 GB

Tpoint	Post Routine Description
28h	Using the table of configurations supplied by the specific chipset module, test each DRAM configuration to see if that particular configuration is valid. Then program the chipset to its autosized configuration. Before autosizing, disable all caches and all shadow RAM.
29h	Initialize the POST Memory Manager
2ah	Zero the first 512K of RAM
2ch	Test 512K base address lines
2eh	Test first 512K of RAM.
2fh	Initialize external cache before shadowing.
32h	Compute CPU speed.
33h	Initialize the Phoenix Dispatch Manager
36h	Vector to proper shutdown routine.
38h	Shadow the system BIOS.
3ah	Autosize external cache and program cache size for enabling later in POST.
3ch	If CMOS is valid, load chipset registers with values from CMOS, otherwise load defaults and display Setup prompt. If Auto Configuration is enabled, always load the chipset registers with the Setup defaults (Rel 6.0).
3dh	Load alternate registers with CMOS values.
41h	Initialize extended memory for RomPilot.
42h	Initialize interrupt vectors 0 thru 77h to the TrustedCore general interrupt handler.

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7.3 Error Codes-3

Tpoint	Post Routine Description
45h	Initialize all motherboard devices.
46h	Verify the ROM copyright notice.
47h	Initialize support for I2O by initializing global variables used by the I2O code. Pause POST table processing if a CMOS bit is set (for debugging).
48h	Verify that the equipment specified in the CMOS matches the hardware currently installed. If the monitor type is set to 00 then a video ROM must exist. If the monitor type is 1 or 2 set the video switch to CGA. If monitor type 3, set the video switch to m
49h	Perform these tasks: 1. Size the PCI bus topology and set bridge bus numbers. 2. Set the system max bus number. 3. Write a 0 to the command register of every PCI device. 4. Write a 0 to all 6 base registers in every PCI device. 5. Write a -1 to the status register of every PCI device. 6. Find all IOPs and initialize them.
4ah	Initialize all video adapters in system.
4bh	Initialize QuietBoot if it is installed. Enable both keyboard and timer interrupts (IRQ0 and IRQ1). If your POST tasks require interrupts off, preserve them with a PUSHF and CLI at the beginning and a POPF at the end. If you change the PIC, preserve the existing bits.
4ch	Shadow video BIOS ROM if specified by Setup, and CMOS is valid and the previous boot was OK.

Tpoint	Post Routine Description
4eh	Display copyright notice.
4fh	Initialize MultiBoot. Allocate memory for old and new MultiBoot history tables.
50h	Display CPU type and speed.
51h	Checksum CMOS and initialize each EISA slot with data from the initialization data block.
52h	Verify keyboard reset.
54h	Initialize keystroke clicker if enabled in Setup.
55h	Enable USB devices.
58h	Test for unexpected interrupts. First do an STI for hot interrupts. Secondly, test the NMI for an unexpected interrupt. Thirdly, enable the parity checkers and read from memory, checking for an unexpected interrupt.
59h	Register POST Display Services, fonts, and languages with the POST Dispatch Manager.
5ah	Display prompt "Press F2 to enter SETUP".
5bh	Disable CPU cache.
5ch	Test RAM between 512K and 640K.
60h	Determine and test the amount of extended memory available. Determine if memory exists by writing to a few strategic locations and see if the data can be read back. If so, perform an address-line test and a RAM test on the memory. Save the total extended

7.3 Error Codes-4

Tpoint	Post Routine Description
62h	Perform an address line test on A0 to the amount of memory available. This test is dependent on the processor, since the test will vary depending on the width of memory (16 or 32 bits). This test will also use A20 as the skew address to prevent corruption
64h	Jump to UserPatch1. See "The POST Component".
66h	Set cache registers to their CMOS values if CMOS is valid, unless auto configuration is enabled, in which case load cache registers from the Setup default table.
67h	Quick initialization of all Application Processors in a multi-processor system.
68h	Enable external cache and CPU cache if present. Configure non-cacheable regions if necessary. NOTE: Hook routine must preserve DX, which carries the cache size to the DisplayCacheSizeJ routine.
69h	Initialize the handler for SMM.
6ah	Display external cache size on the screen if it is non-zero. NOTE: Hook routine must preserve DX, which carries the cache size from the cacheConfigureJ routine.
6bh	If CMOS is bad, load Custom Defaults from flash into CMOS. If successful, reboot.
6ch	Display shadow message.
6eh	Display the starting offset of the nondisposable segment of TrustedCore.
70h	Check flags in CMOS and in the TrustedCore data area for errors detected during POST. Display error messages on the screen.

Tpoint	Post Routine Description
72h	Check status bits to see if configuration problems were detected. If so, display error messages on the screen.
76h	Check status bits for keyboard-related failures. Display error messages on the screen.
7ch	Initialize the hardware interrupt vectors from 08 to 0F and from 70h to 77H. Also set the interrupt vectors from 60h to 66H to zero.
7dh	Initialize Intelligent System Monitoring.
7eh	The Coprocessor initialization test. Use the floating point instructions to determine if a coprocessor exists instead of the ET bit in CR0.
80h	Disable onboard COM and LPT ports before testing for presence of external I/O devices.
81h	Run late device initialization routines.
82h	Test and identify RS232 ports.
83h	Configure Fisk Disk Controller.
84h	Test and identify parallel ports.
85h	Display any ESCD read errors and configure all PnP ISA devices.
86h	Initialize onboard I/O and BDA according to CMOS and presence of external devices.
87h	Initialize motherboard configurable devices.
88h	Initialize interrupt controller.
89h	Enable non-maskable interrupts.
8ah	Initialize Extended BIOS Data Area and initialize the mouse.
8bh	Setup interrupt vector and present bit in Equipment byte.

7.3 Error Codes-5

Tpoint	Post Routine Description
8ch	Initialize both of the floppy disks and display an error message if failure was detected. Check both drives to establish the appropriate diskette types in the TrustedCore data area.
8fh	Count the number of ATA drives in the system and update the number in bdaFdiskcount.
90h	Initialize hard-disk controller. If the CMOS ram is valid and intact, and fixed disks are defined, call the fixed disk init routine to initialize the fixed disk system and take over the appropriate interrupt vectors.
91h	Configure the local bus IDE timing register based on the drives attached to it.
92h	Jump to UserPatch2. See "The POST Component".
93h	Build the MPTABLE for multi-processor boards.
95h	1. Check CMOS for CD-ROM drive present. 2. Activate the drive by checking for media present. 3. Check sector 11h (17) for Boot Record Volume Descriptor. 4. Check the boot catalog for validity. 5. Pick a boot entry. 6. Create a Specification Packet.
96h	Reset segment-register addressibility from 4GB to normal 64K by generating a Shutdown 8.
97h	Create pointer to MP table in Extended BDA.
98h	Search for option ROMs. Rom scan the area from C800h for a length of BCP_ROM_Scan_Size (or to E000h by default) on every 2K boundary, looking for add on cards that need initialization.

Tpoint	Post Routine Description
99h	Check support status for Self-Monitoring Analysis Reporting Technology (disk-failure warning).
9ah	Shadow miscellaneous ROMs if specified by Setup and CMOS is valid and the previous boot was OK.
9ch	Set up Power Management. Initiate power -management state machine.
9dh	Initialize Security Engine.
9eh	Enable hardware interrupts.
9fh	Check the total number of Fast Disks (ATA and SCSI) and update the bdaFdiskCount.
a0h	Verify that the system clock is interrupting.
a2h	Setup Numlock indicator. Display a message if key switch is locked.
a4h	Initialize typematic rate.
a8h	Overwrite the "Press F2 for Setup" prompt with spaces, erasing it from the screen.
aah	Scan the key buffer to see if the F2 key was struck after keyboard interrupts were enabled. If an F2 keystroke is found, set a flag.

7.3 Error Codes-6

Tpoint	Post Routine Description

ach	Enter SETUP.
	If (F2 was pressed)
	go to SETUP
	Else if (errors were found)
	display "Press F1 or F2" prompt
	if (F2 is pressed)
	go to setup
	else if (F1 is pressed)
	boot
	Else boot

aeh	Clear ConfigFailedBit and InPostBit in CMOS.

b0h	Check for errors.
	If (errors were found)
	beep twice
	display "F1 or F2" message
	if (F2 keystroke) go to SETUP
	if (F1 keystroke) go to BOOT

b1h	Inform RomPilot about the end of POST.
b2h	Change status bits in CMOS and/or the TrustedCore data area to reflect the fact that POST is complete.
b4h	One quick beep

Tpoint	Post Routine Description

b5h	Turn off <Esc> and <F2> key checking.
	IF (VGA adapter is present)
	IF (OEM screen is still up)
	Note OEM screen is gone.
	Fade out OEM screen.
	Reset video: clear screen, reset cursor, reload DAC.
	ENDIF
	ENDIF

b6h	If password on boot is enabled, a call is made to Setup to check password. If the user does not enter a valid password, Setup does not return.
b7h	Initialize ACPI BIOS.
b9h	Clear all screen graphics before booting.
bah	Initialize the SMBIOS header and substructures.
bch	Clear parity-error latch
bdh	Display Boot First menu if MultiBoot is installed.
beh	If BCP option is enabled, clear the screen before booting.
bfh	Check virus and backup reminders. Display System Summary.
c0h	Try to boot with INT 19
c1h	Initialize the Post Error Manager.

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7.3 Error Codes-7

Tpoint	Post Routine Description
c2h	Write PEM errors.
c3h	Display PEM errors.
c4h	Initialize system error handler
c5h	PnPnd dual CMOS (optional)
c6h	Initialize note dock
c7h	Initialize note dock late
c8h	Force check (optional)
c9h	Extended checksum (optional)
cah	Redirect Int 15h to enable target board to use remote keyboard (PICO BIOS).
cbh	Redirect Int 13h to Memory Technologies Devices such as ROM,RAM, PCMCIA, and serial disk (PICO BIOS).
cch	Redirect Int 10h to enable target board to use a remote serial video (PICO BIOS).
cdh	Remap I/O and memory address space for PCMCIA (PICO BIOS).
ceh	Initialize digitizer device and display installed message if successful.
d2h	Unknown interrupt The following are for Boot Block in Flash The following are for Boot Block in FlashROM.
e0h	Initialize the chipset
e1h	Initialize the bridge
e2h	Initialize the CPU
e3h	Initialize system timer
e4h	Initialize system I/O

Tpoint	Post Routine Description
e5h	Check force recovery boot
e6h	Checksum BIOS ROM
e7h	Go to TrustedCore
e8h	Initialize Multi Processor
e9h	Set Huge Segment
eah	Initialilze OEM special code
ebh	Initialize PIC and DMA
ech	Initialize Memory type
edh	Initialize Memory size
eeh	Shadow Boot Block
efh	System memory test
f0h	Initialize interrupt vectors
f1h	Initialize Run Time Clock
f2h	Initialize video
f3h	Initialize System Management Mode
f4h	Output one beep
f5h	Boot to Mini DOS
f6h	Clear Huge segment
f7h	Boot to Full DOS

8. Trouble Shooting

- ☐ 8.1 No Power (*1)
- ☐ 8.2 No Display (*2)
- ☐ 8.3 VGA Controller Test Error LCD No Display
- ☐ 8.4 External Monitor No Display or Color Abnormal
- ☐ 8.5 Memory Test Error
- ☐ 8.6 Keyboard (K/B) or Touch Pad (T/P) Test Error
- ☐ 8.7 Hard Disk Drive Test Error
- ☐ 8.8 CD-ROM Test Error
- ☐ 8.9 USB Port Test Error
- ☐ 8.10 Audio Test Error
- ☐ 8.11 LAN Test Error
- ☐ 8.12 1394B Test Error
- ☐ 8.13 Mini Express (wireless) Socket Test Error
- ☐ 8.14 PCMCIA Socket Test Error

*1: No Power Definition

Base on ACPI Spec, We define no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display.

Base on these three conditions to analyze the schematic and edit the no display chapter.

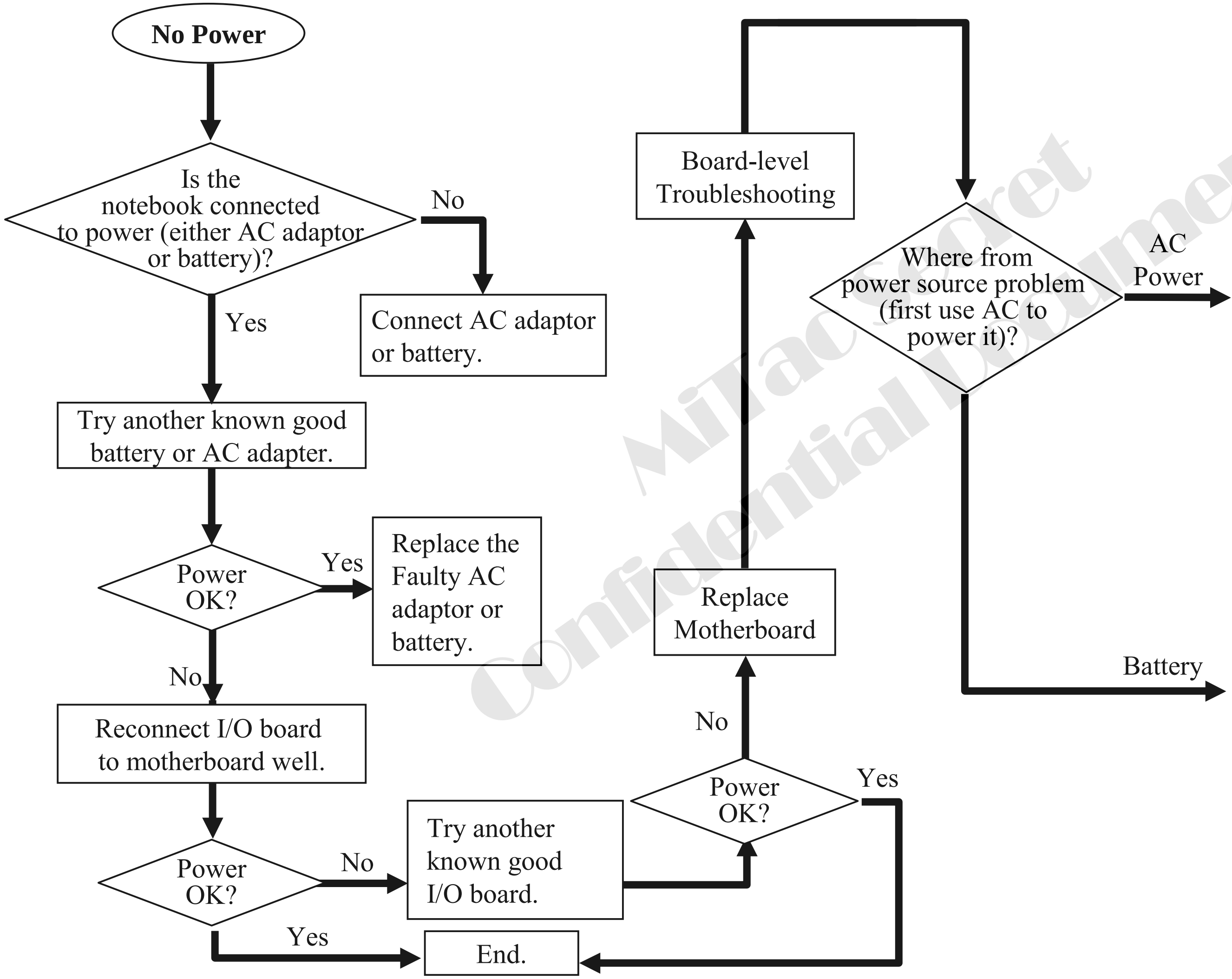
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification.

8.1 No Power-1

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.


No Power
Is the notebook connected to power (either AC adaptor or battery)?
No
Connect AC adaptor or battery.
Yes
Try another known good battery or AC adapter.
Power OK?
Yes
Replace the Faulty AC adaptor or battery.
No
Reconnect I/O board to motherboard well.
Power OK?
No
Try another known good I/O board.
Yes
End.
Power OK?
Yes
No
Replace Motherboard
Board-level Troubleshooting
Where from power source problem (first use AC to power it)?
AC Power
Battery

Check following parts and signals:

Parts

PJ1
PL505
PF501
PF502
PQ3
PQ518
PQ519
PQ521
PQ523
PU506
PQ526~PQ528
PD501~PD504
PL501~PL503
PD519~PD522

Signals

Vsys
VDOCK
ADINP
LEARNING#
ADEN#
PWR_AC
CHG_A#
CHG_B#

Check following parts and signals:

Parts:

PJ2
PJ3
PU4
PQ522
PQ533
PQ534
PF502
PF503
PF504

Signals:

ABATT+/BBATT+
VBATT1/2
PWR_BATT#
DCH_A/B#
SMC_A/B
SMD_A/B
BAT_CLK/DATA

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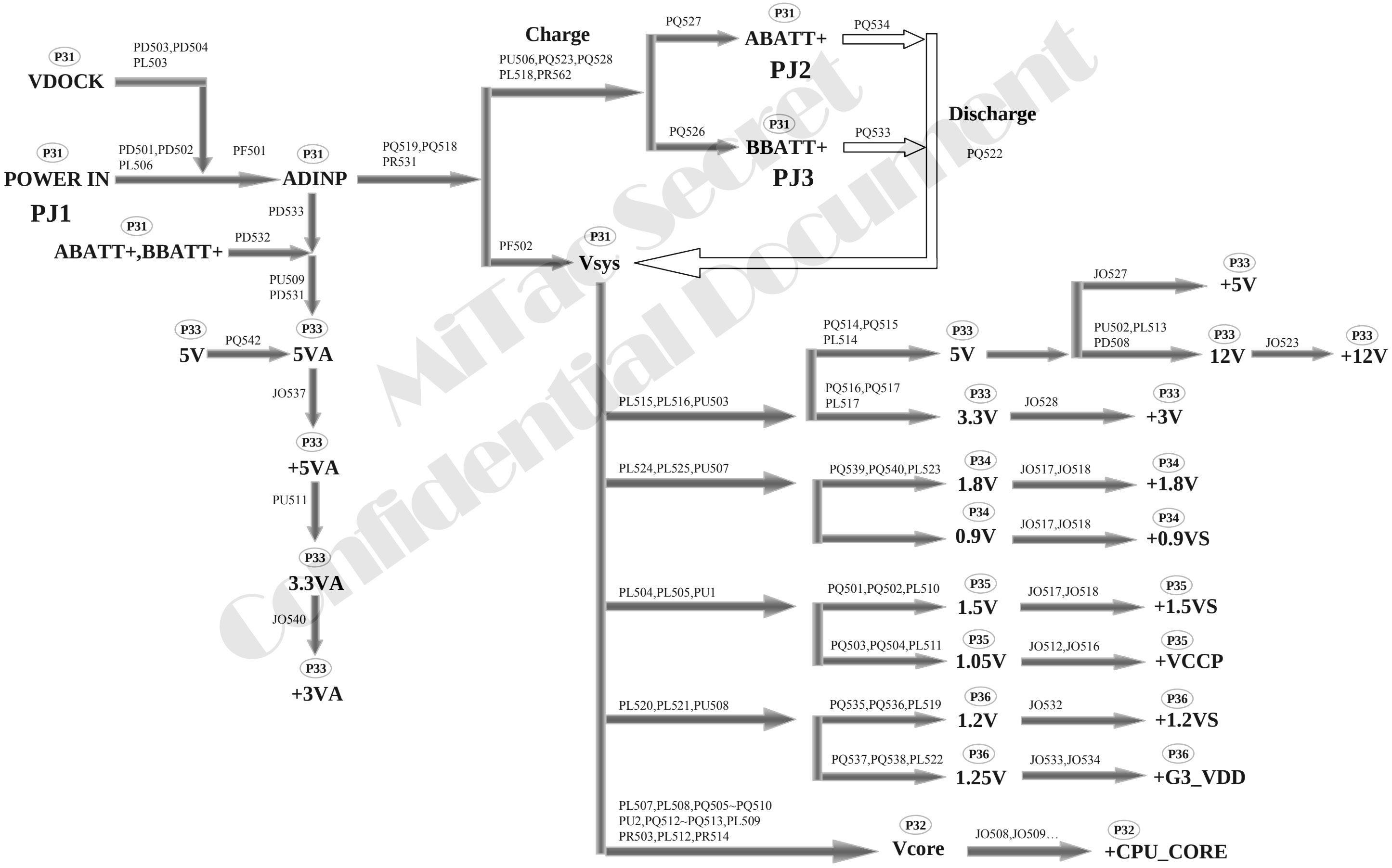
M230 N/B Maintenance

8.1 No Power-2

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map


P31
VDOCK
PD503,PD504
PL503
P31
POWER IN
PJ1
PD501,PD502
PL506
PF501
P31
ADINP
PD533
P31
ABATT+,BBATT+
PD532
PU509
PD531
P33
5V
PQ542
P33
5VA
JO537
P33
+5VA
PU511
P33
3.3VA
JO540
P33
+3VA
PQ519,PQ518
PR531
Charge
PU506,PQ523,PQ528
PL518,PR562
PQ527
P31
ABATT+
PJ2
PQ534
PQ526
P31
BBATT+
PJ3
PQ533
Discharge
PQ522
PF502
P31
Vsys
JO527
P33
+5V
PQ514,PQ515
PL514
P33
5V
PU502,PL513
PD508
P33
12V
JO523
P33
+12V
PL515,PL516,PU503
PQ516,PQ517
PL517
P33
3.3V
JO528
P33
+3V
PL524,PL525,PU507
PQ539,PQ540,PL523
P34
1.8V
JO517,JO518
P34
+1.8V
P34
0.9V
JO517,JO518
P34
+0.9VS
PL504,PL505,PU1
PQ501,PQ502,PL510
P35
1.5V
JO517,JO518
P35
+1.5VS
PQ503,PQ504,PL511
P35
1.05V
JO512,JO516
P35
+VCCP
PL520,PL521,PU508
PQ535,PQ536,PL519
P36
1.2V
JO532
P36
+1.2VS
PQ537,PQ538,PL522
P36
1.25V
JO533,JO534
P36
+G3_VDD
PL507,PL508,PQ505~PQ510
PU2,PQ512~PQ513,PL509
PR503,PL512,PR514
P32
Vcore
JO508,JO509…
P32
+CPU_CORE

NOTE :

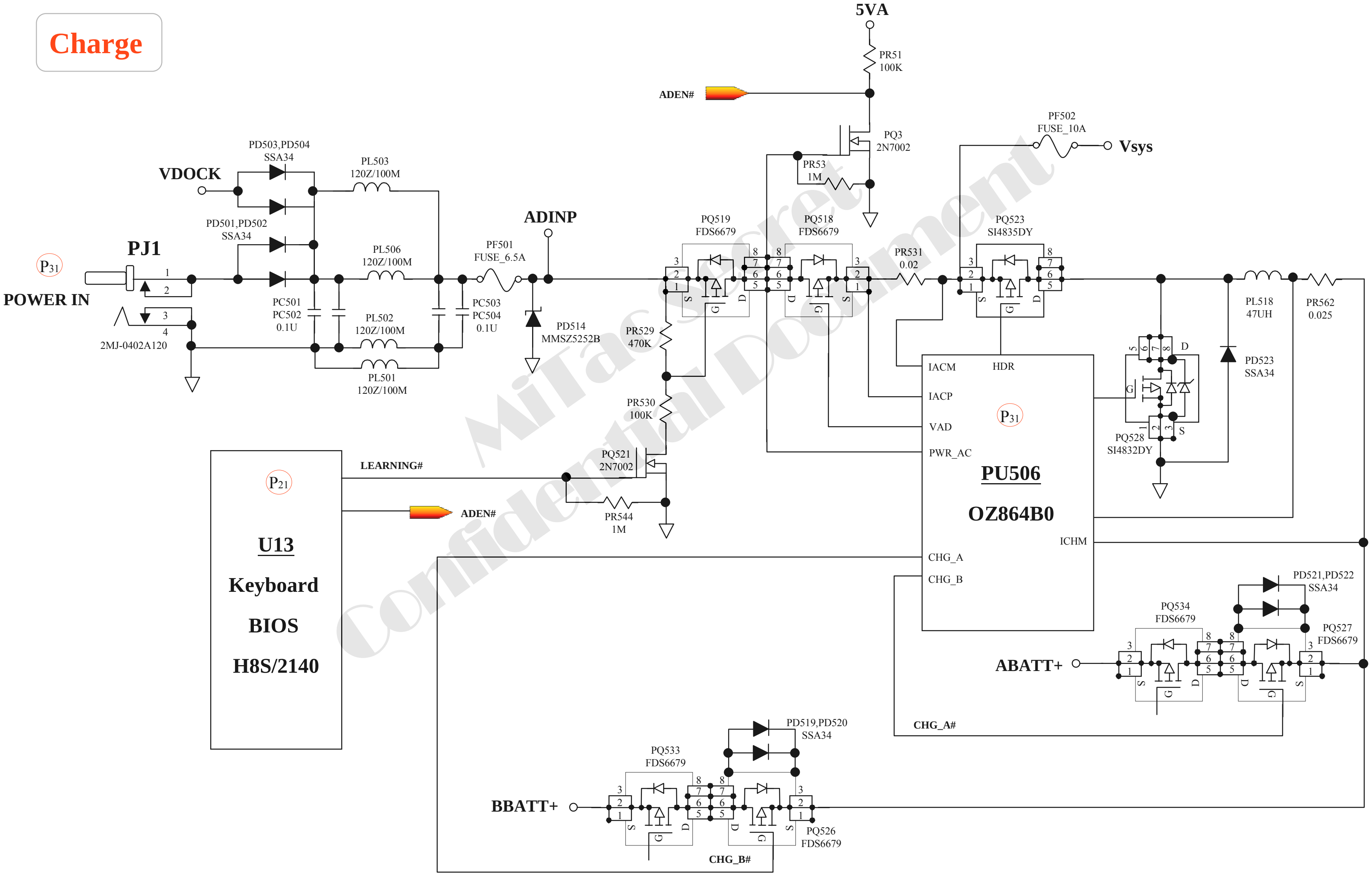
P33 : Page 33 on M/B Board circuit diagram.

M230 N/B Maintenance

8.1 No Power-3

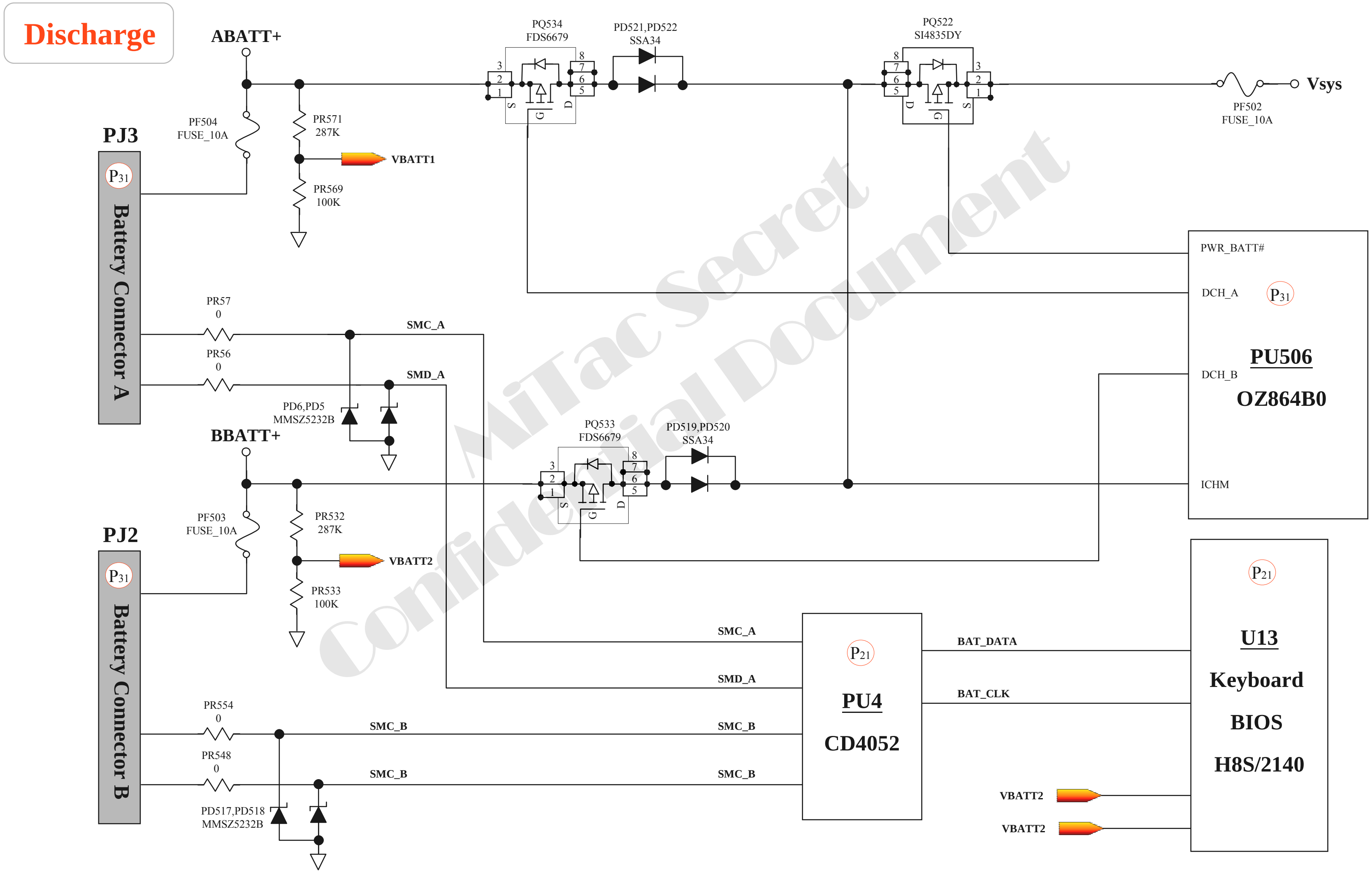
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Charge


5VA
PR51
100K
ADEN#
PQ3
2N7002
PR53
1M
PF502
FUSE_10A
Vsys
PD503,PD504
SSA34
VDOCK
PL503
120Z/100M
PD501,PD502
SSA34
ADINP
PJ1
P31
POWER IN
1
2
3
4
2MJ-0402A120
PL506
120Z/100M
PF501
FUSE_6.5A
PC501
PC502
0.1U
PL502
120Z/100M
PC503
PC504
0.1U
PL501
120Z/100M
PD514
MMSZ5252B
PQ519
FDS6679
PQ518
FDS6679
PR531
0.02
PQ523
SI4835DY
PL518
47UH
PR562
0.025
PR529
470K
PR530
100K
IACM
HDR
IACP
VAD
PWR_AC
P31
PU506
OZ864B0
ICHM
CHG_A
CHG_B
PD523
SSA34
PQ528
SI4832DY
P21
U13
Keyboard
BIOS
H8S/2140
LEARNING#
PQ521
2N7002
ADEN#
PR544
1M
PD521,PD522
SSA34
PQ534
FDS6679
PQ527
FDS6679
ABATT+
CHG_A#
PD519,PD520
SSA34
PQ533
FDS6679
BBATT+
PQ526
FDS6679
CHG_B#
S
G
D

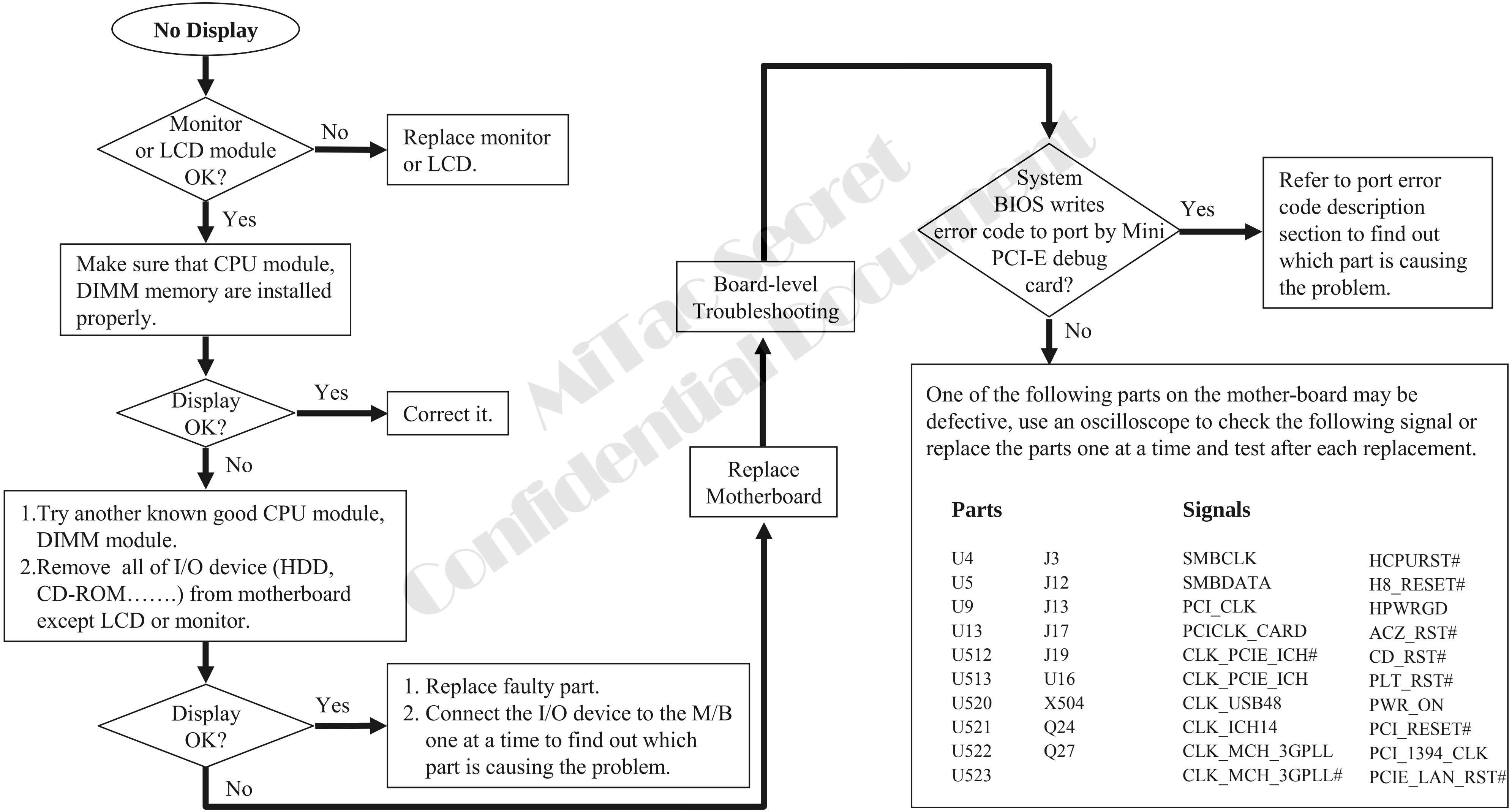
8.1 No Power-4

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.


Discharge
ABATT+
PQ534
FDS6679
PD521,PD522
SSA34
PQ522
SI4835DY
Vsys
PF502
FUSE_10A
PJ3
P31
Battery Connector A
PF504
FUSE_10A
PR571
287K
VBATT1
PR569
100K
PWR_BATT#
DCH_A
P31
PU506
OZ864B0
DCH_B
ICHM
PR57
0
SMC_A
PR56
0
SMD_A
PD6,PD5
MMSZ5232B
BBATT+
PQ533
FDS6679
PD519,PD520
SSA34
PJ2
P31
Battery Connector B
PF503
FUSE_10A
PR532
287K
VBATT2
PR533
100K
SMC_A
SMD_A
P21
PU4
CD4052
BAT_DATA
BAT_CLK
P21
U13
Keyboard
BIOS
H8S/2140
PR554
0
SMC_B
SMC_B
PR548
0
SMC_B
SMC_B
PD517,PD518
MMSZ5232B
VBATT2
VBATT2

8.2 No Display-1

There is no display on both LCD and monitor after power on although the LCD and monitor is known-good.


No Display
Monitor or LCD module OK?
No
Replace monitor or LCD.
Yes
Make sure that CPU module, DIMM memory are installed properly.
Display OK?
Yes
Correct it.
No
1.Try another known good CPU module, DIMM module.
2.Remove all of I/O device (HDD, CD-ROM…….) from motherboard except LCD or monitor.
Display OK?
Yes
1. Replace faulty part.
2. Connect the I/O device to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting
System BIOS writes error code to port by Mini PCI-E debug card?
Yes
Refer to port error code description section to find out which part is causing the problem.
No

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts		**Signals**	
U4	J3	SMBCLK	HCPURST#
U5	J12	SMBDATA	H8_RESET#
U9	J13	PCI_CLK	HPWRGD
U13	J17	PCICLK_CARD	ACZ_RST#
U512	J19	CLK_PCIE_ICH#	CD_RST#
U513	U16	CLK_PCIE_ICH	PLT_RST#
U520	X504	CLK_USB48	PWR_ON
U521	Q24	CLK_ICH14	PCI_RESET#
U522	Q27	CLK_MCH_3GPLL	PCI_1394_CLK
U523		CLK_MCH_3GPLL#	PCIE_LAN_RST#

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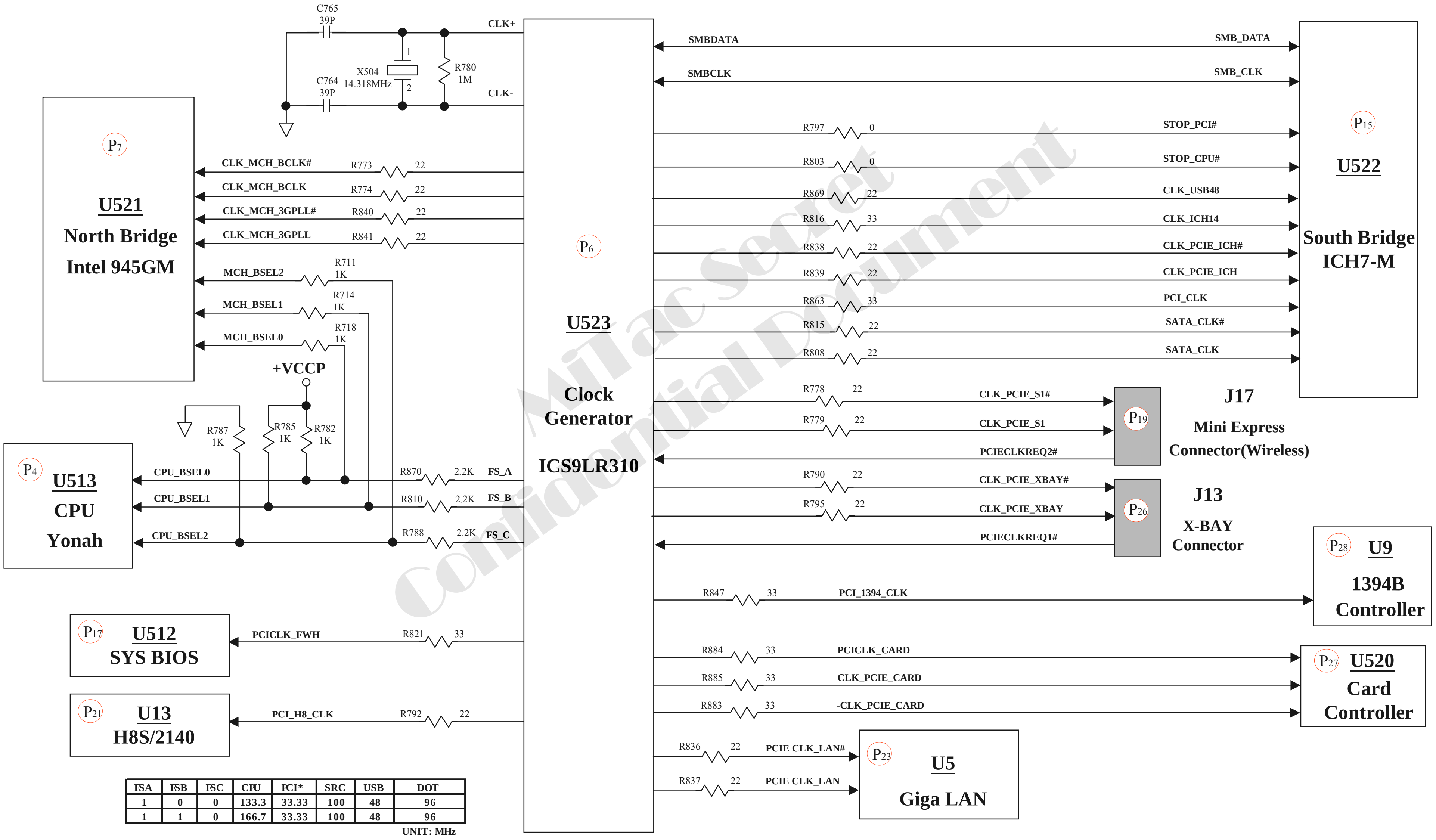
M230 N/B Maintenance

8.2 No Display-2

****** System Clock Check ******


C765
39P
CLK+
X504
14.318MHz
1
2
R780
1M
C764
39P
CLK-
P7
U521
North Bridge
Intel 945GM
CLK_MCH_BCLK#
R773 22
CLK_MCH_BCLK
R774 22
CLK_MCH_3GPLL#
R840 22
CLK_MCH_3GPLL
R841 22
MCH_BSEL2
R711 1K
MCH_BSEL1
R714 1K
MCH_BSEL0
R718 1K
+VCCP
R787 1K
R785 1K
R782 1K
P4
U513
CPU
Yonah
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
R870 2.2K FS_A
R810 2.2K FS_B
R788 2.2K FS_C
P17
U512
SYS BIOS
PCICLK_FWH
R821 33
P21
U13
H8S/2140
PCI_H8_CLK
R792 22
P6
U523
Clock
Generator
ICS9LR310
SMBDATA
SMB_DATA
SMBCLK
SMB_CLK
R797 0 STOP_PCI#
R803 0 STOP_CPU#
R869 22 CLK_USB48
R816 33 CLK_ICH14
R838 22 CLK_PCIE_ICH#
R839 22 CLK_PCIE_ICH
R863 33 PCI_CLK
R815 22 SATA_CLK#
R808 22 SATA_CLK
P15
U522
South Bridge
ICH7-M
R778 22 CLK_PCIE_S1#
R779 22 CLK_PCIE_S1
PCIECLKREQ2#
P19
J17
Mini Express
Connector(Wireless)
R790 22 CLK_PCIE_XBAY#
R795 22 CLK_PCIE_XBAY
PCIECLKREQ1#
P26
J13
X-BAY
Connector
R847 33 PCI_1394_CLK
P28
U9
1394B
Controller
R884 33 PCICLK_CARD
R885 33 CLK_PCIE_CARD
R883 33 -CLK_PCIE_CARD
P27
U520
Card
Controller
R836 22 PCIE CLK_LAN#
R837 22 PCIE CLK_LAN
P23
U5
Giga LAN

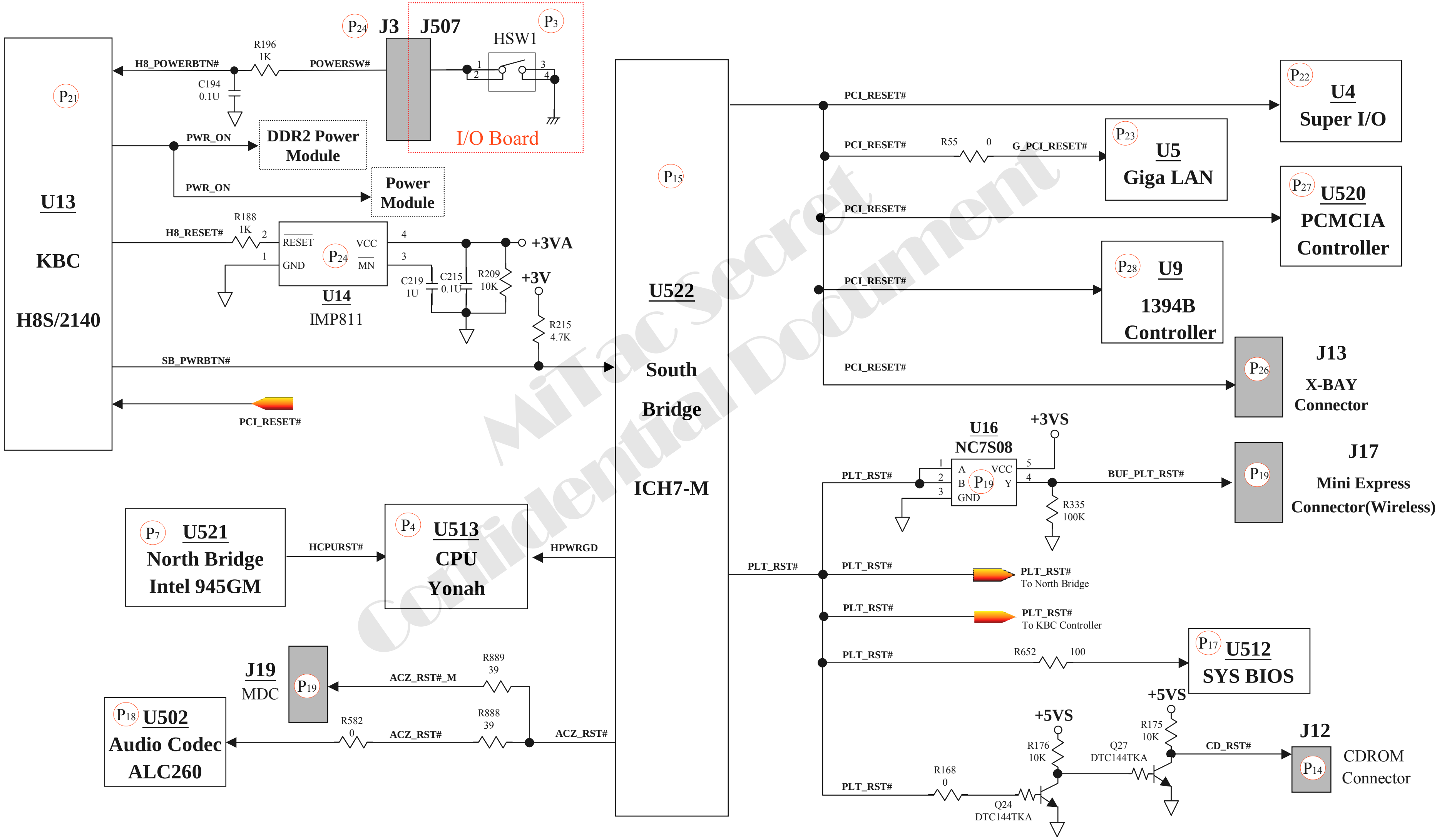
FSA	FSB	FSC	CPU	PCI*	SRC	USB	DOT
1	0	0	133.3	33.33	100	48	96
1	1	0	166.7	33.33	100	48	96

UNIT: MHz

M230 N/B Maintenance

8.2 No Display-3

****** Power Good & Reset Circuit Check ******



P21
U13
KBC
H8S/2140
H8_POWERBTN#
R196
1K
POWERSW#
C194
0.1U
P24
J3
J507
P3
HSW1
1
2
3
4
I/O Board
PWR_ON
DDR2 Power Module
PWR_ON
Power Module
R188
1K
H8_RESET#
2
1
RESET
GND
P24
VCC
MN
4
3
+3VA
U14
IMP811
C219
1U
C215
0.1U
R209
10K
+3V
R215
4.7K
SB_PWRBTN#
PCI_RESET#
P15
U522
South Bridge
ICH7-M
PCI_RESET#
P22
U4
Super I/O
PCI_RESET#
R55
0
G_PCI_RESET#
P23
U5
Giga LAN
PCI_RESET#
P27
U520
PCMCIA Controller
PCI_RESET#
P28
U9
1394B Controller
PCI_RESET#
P26
J13
X-BAY Connector
U16
NC7S08
+3VS
PLT_RST#
1
2
3
A
B
GND
P19
VCC
Y
5
4
BUF_PLT_RST#
R335
100K
P19
J17
Mini Express Connector(Wireless)
P7
U521
North Bridge
Intel 945GM
HCPURST#
P4
U513
CPU
Yonah
HPWRGD
PLT_RST#
PLT_RST#
PLT_RST#
To North Bridge
PLT_RST#
PLT_RST#
To KBC Controller
PLT_RST#
R652
100
P17
U512
SYS BIOS
J19
MDC
P19
R889
39
ACZ_RST#_M
P18
U502
Audio Codec
ALC260
R582
0
ACZ_RST#
R888
39
ACZ_RST#
+5VS
+5VS
R175
10K
R176
10K
Q27
DTC144TKA
CD_RST#
J12
P14
CDROM Connector
R168
0
PLT_RST#
Q24
DTC144TKA

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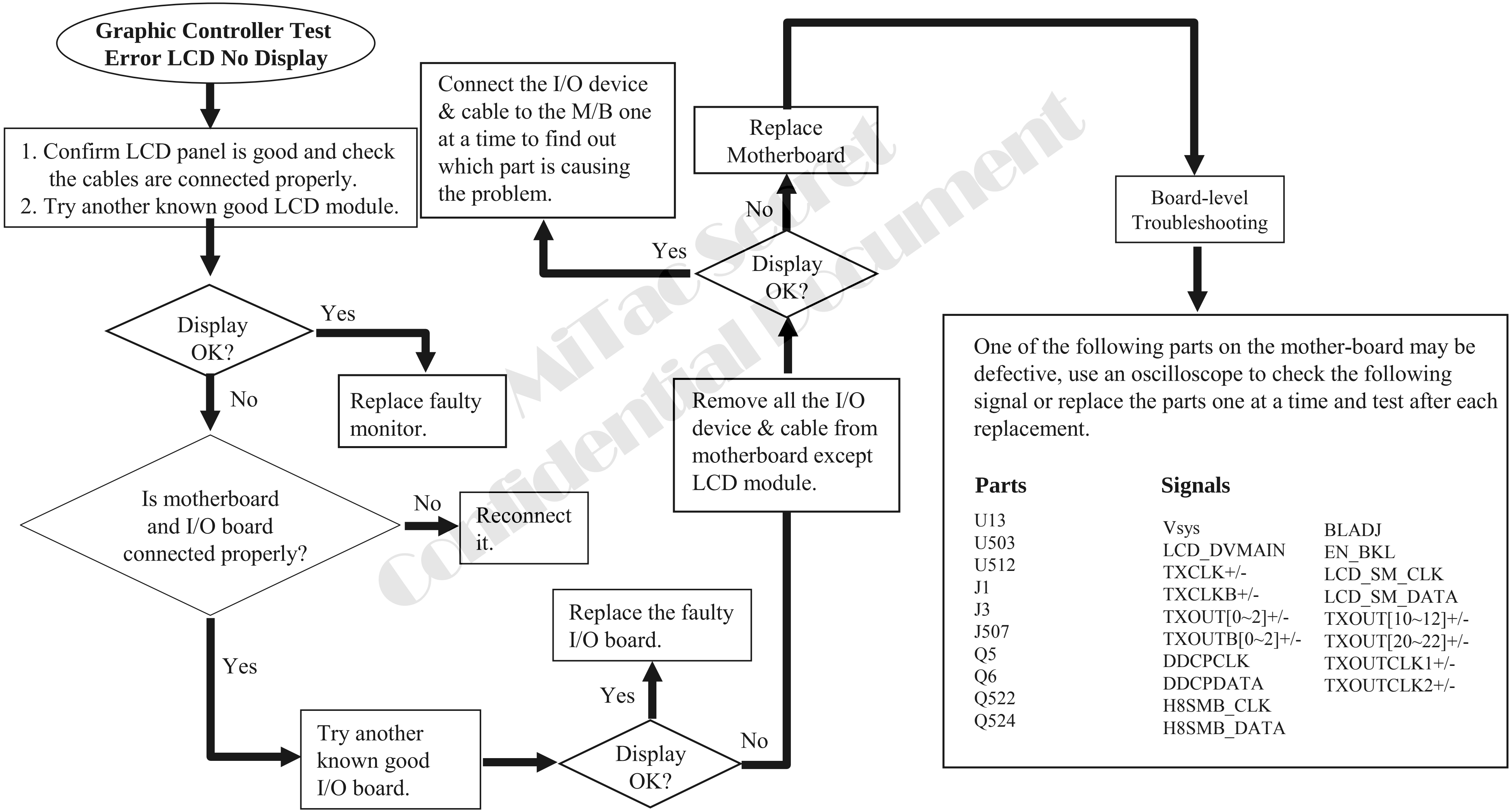
8.3 Graphic Controller Test Error LCD No Display-1

There is no display or picture abnormal on LCD although power-on-self-test is passed.


Graphic Controller Test Error LCD No Display
1. Confirm LCD panel is good and check the cables are connected properly.
2. Try another known good LCD module.
Display OK?
Yes
Replace faulty monitor.
No
Is motherboard and I/O board connected properly?
No
Reconnect it.
Yes
Try another known good I/O board.
Display OK?
Yes
Replace the faulty I/O board.
No
Remove all the I/O device & cable from motherboard except LCD module.
Display OK?
Yes
Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts

U13
U503
U512
J1
J3
J507
Q5
Q6
Q522
Q524

Signals

Vsys
LCD_DVMAIN
TXCLK+/-
TXCLKB+/-
TXOUT[0~2]+/-
TXOUTB[0~2]+/-
DDCPCLK
DDCPDATA
H8SMB_CLK
H8SMB_DATA

BLADJ
EN_BKL
LCD_SM_CLK
LCD_SM_DATA
TXOUT[10~12]+/-
TXOUT[20~22]+/-
TXOUTCLK1+/-
TXOUTCLK2+/-

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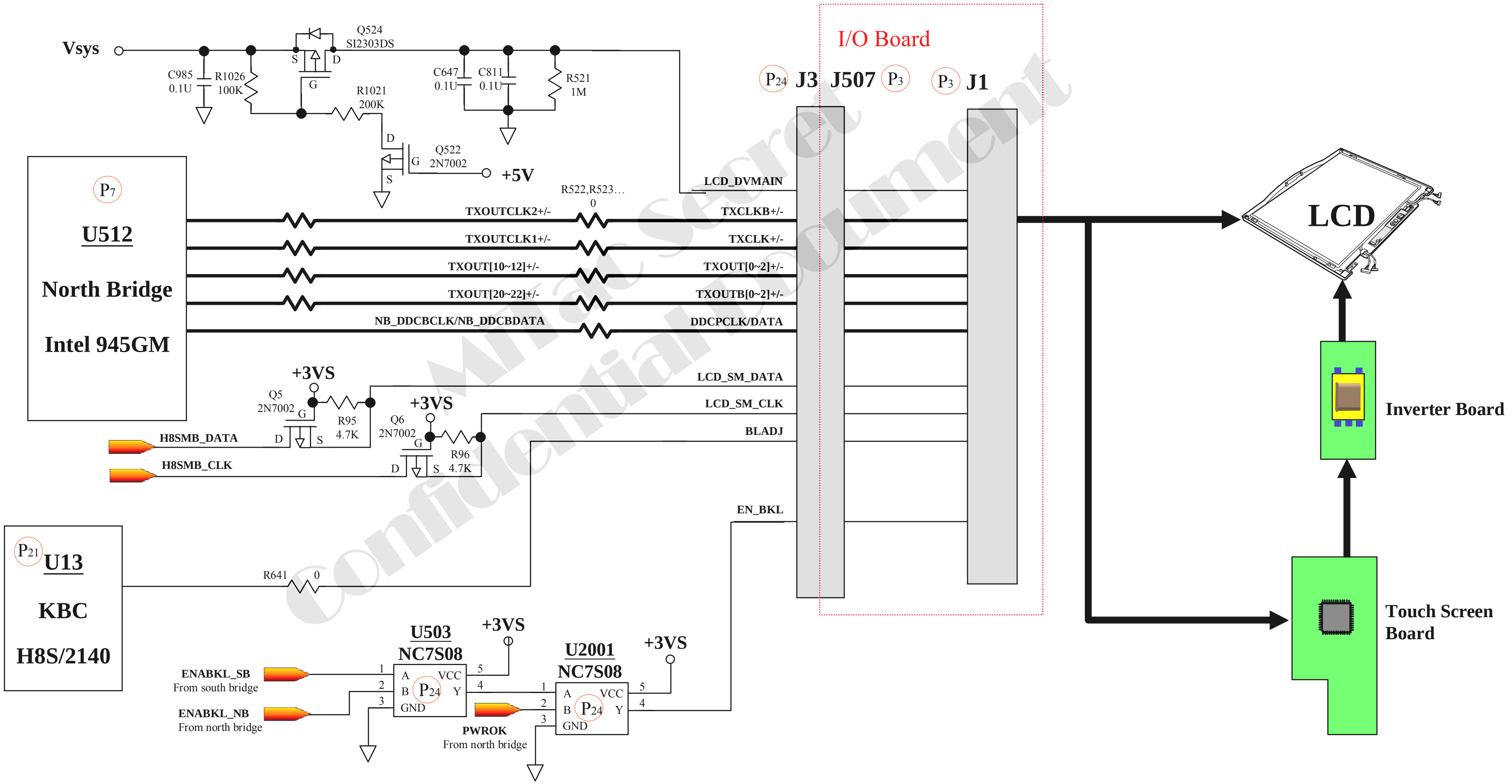
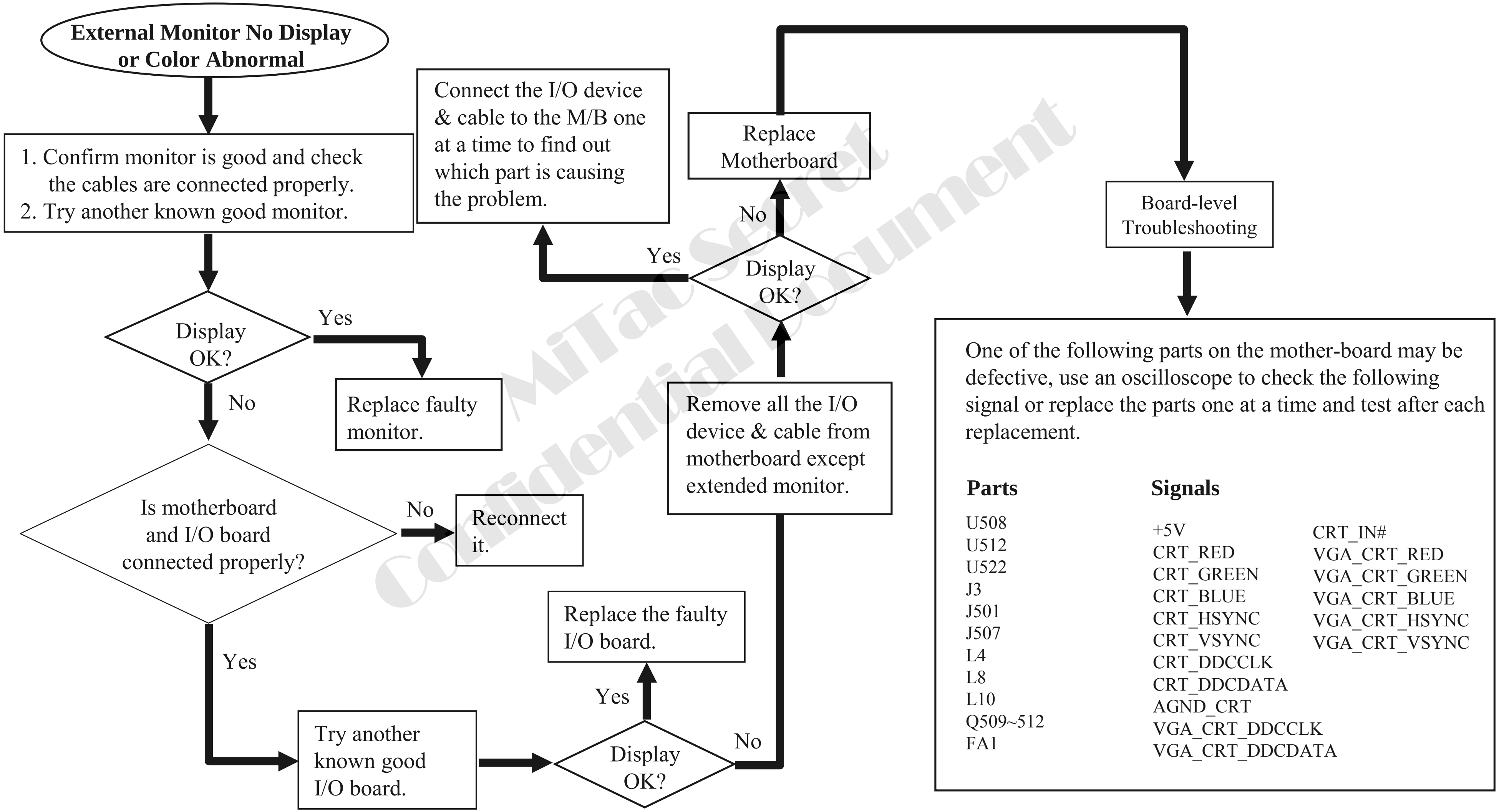
8.3 Graphic Controller Test Error LCD No Display-2

There is no display or picture abnormal on LCD although power-on-self-test is passed.


Vsys
C985
0.1U
R1026
100K
Q524
SI2303DS
S
D
G
R1021
200K
C647
0.1U
C811
0.1U
R521
1M
D
Q522
2N7002
G
S
+5V
I/O Board
P24
J3
J507
P3
P3
J1
LCD_DVMAIN
R522,R523…
0
P7
U512
North Bridge
Intel 945GM
TXOUTCLK2+/-
TXCLKB+/-
TXOUTCLK1+/-
TXCLK+/-
TXOUT[10~12]+/-
TXOUT[0~2]+/-
TXOUT[20~22]+/-
TXOUTB[0~2]+/-
NB_DDCBCLK/NB_DDCBDATA
DDCPCLK/DATA
+3VS
Q5
2N7002
G
R95
4.7K
+3VS
Q6
2N7002
G
R96
4.7K
LCD_SM_DATA
LCD_SM_CLK
BLADJ
H8SMB_DATA
D
S
H8SMB_CLK
D
S
EN_BKL
P21
U13
KBC
H8S/2140
R641
0
U503
NC7S08
+3VS
ENABKL_SB
From south bridge
ENABKL_NB
From north bridge
1
2
3
A
B
GND
VCC
Y
P24
5
4
U2001
NC7S08
+3VS
PWROK
From north bridge
1
2
3
A
B
GND
VCC
Y
P24
5
4
LCD
Inverter Board
Touch Screen
Board

8.4 External Monitor No Display or Color Abnormal-1

There is no display or picture abnormal on monitor.


External Monitor No Display or Color Abnormal
1. Confirm monitor is good and check the cables are connected properly.
2. Try another known good monitor.
Display OK?
Yes
Replace faulty monitor.
No
Is motherboard and I/O board connected properly?
No
Reconnect it.
Yes
Try another known good I/O board.
Display OK?
Yes
Replace the faulty I/O board.
No
Remove all the I/O device & cable from motherboard except extended monitor.
Display OK?
Yes
Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts

U508
U512
U522
J3
J501
J507
L4
L8
L10
Q509~512
FA1

Signals

+5V
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_HSYNC
CRT_VSYNC
CRT_DDCCLK
CRT_DDCDATA
AGND_CRT
VGA_CRT_DDCCLK
VGA_CRT_DDCDATA

CRT_IN#
VGA_CRT_RED
VGA_CRT_GREEN
VGA_CRT_BLUE
VGA_CRT_HSYNC
VGA_CRT_VSYNC

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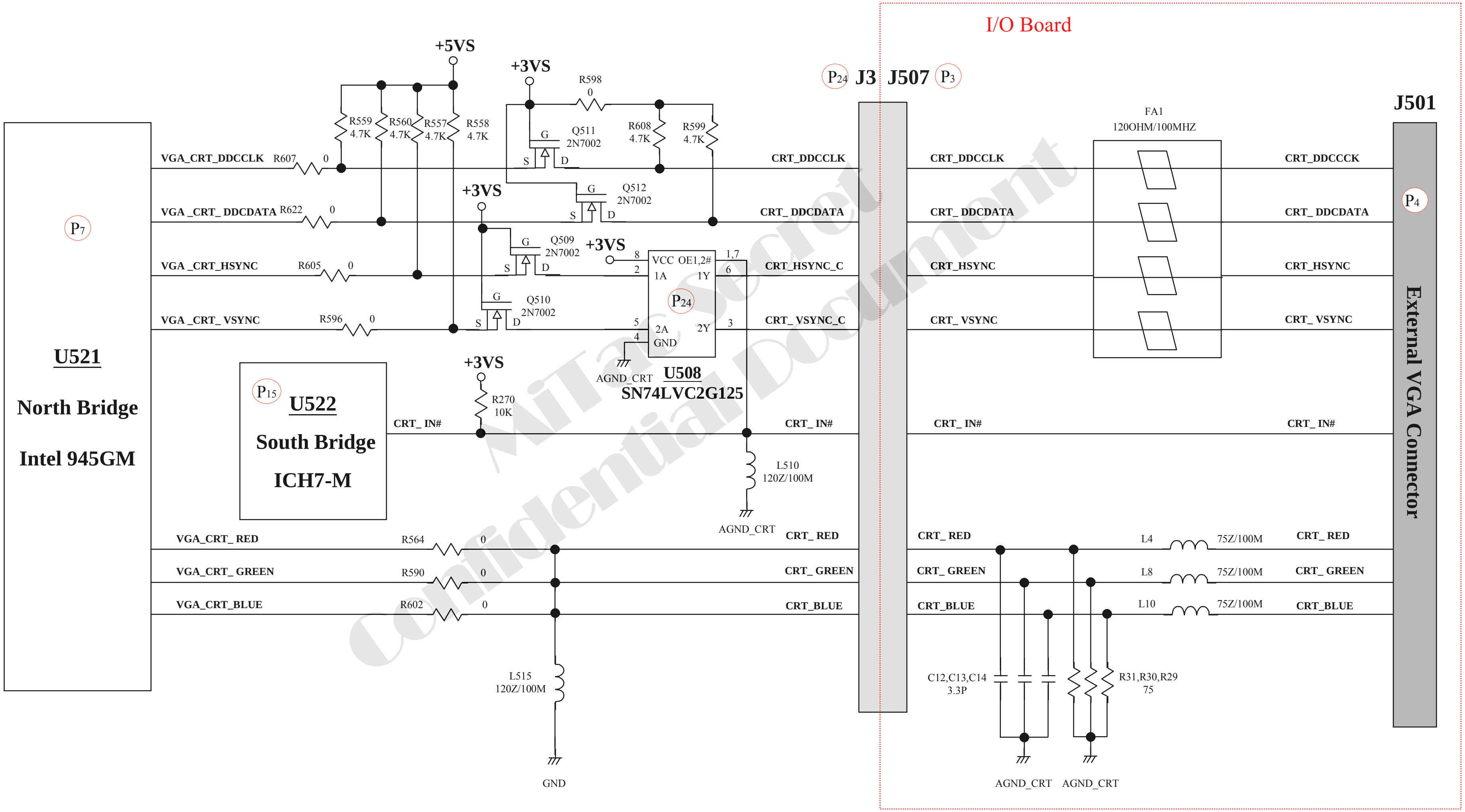
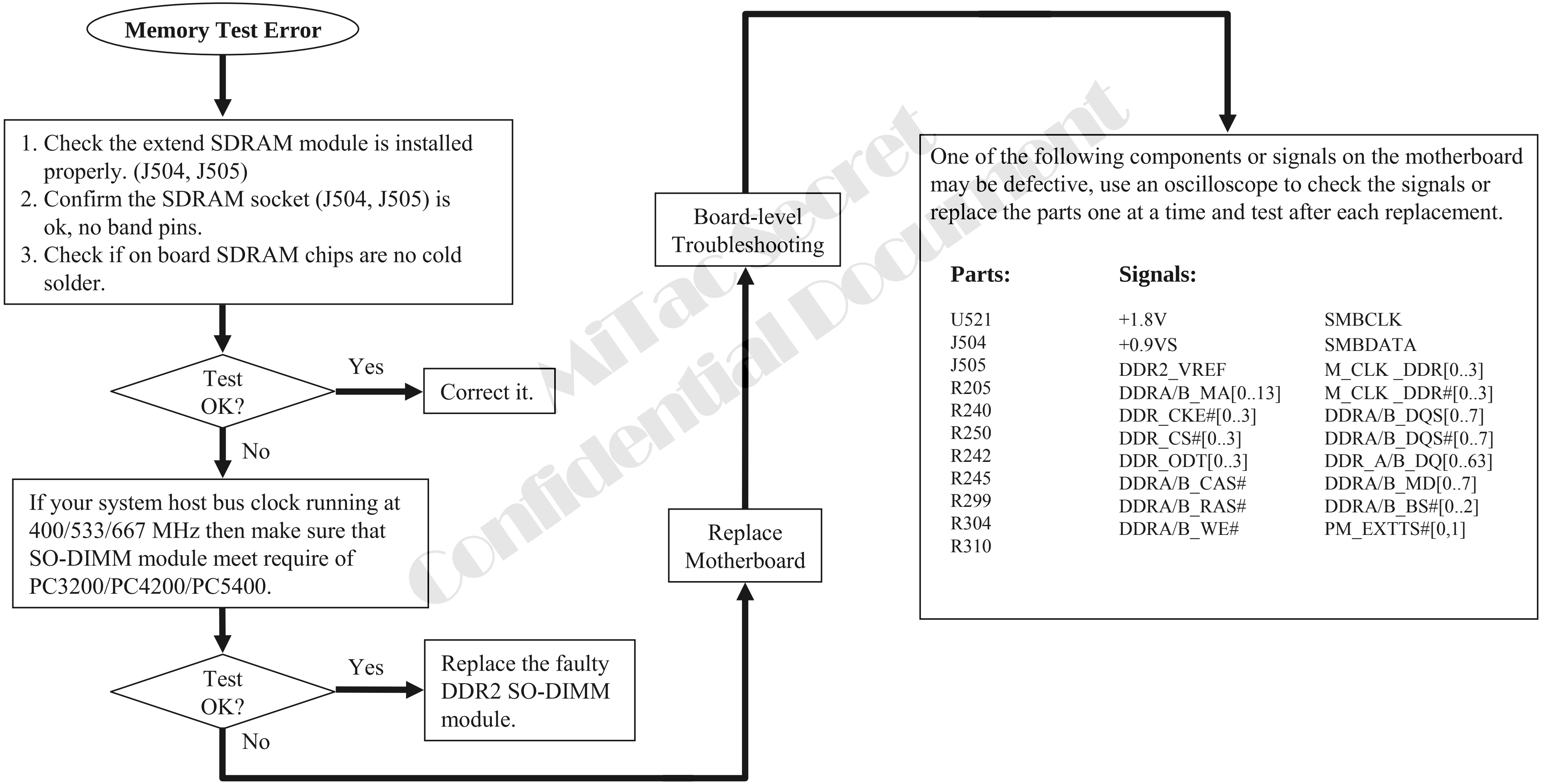
8.4 External Monitor No Display or Color Abnormal-2

There is no display or picture abnormal on monitor.


I/O Board
+5VS
+3VS
R598
0
P24 J3 J507 P3
J501
R559
4.7K
R560
4.7K
R557
4.7K
R558
4.7K
G
Q511
2N7002
S
D
R608
4.7K
R599
4.7K
FA1
120OHM/100MHZ
VGA_CRT_DDCCLK
R607
0
CRT_DDCCLK
CRT_DDCCLK
CRT_DDCCCK
G
Q512
2N7002
S
D
+3VS
P4
P7
VGA _CRT_ DDCDATA
R622
0
CRT_ DDCDATA
CRT_ DDCDATA
CRT_ DDCDATA
G
Q509
2N7002
S
D
+3VS
8
VCC OE1,2#
1,7
2
1A
1Y
6
VGA _CRT_HSYNC
R605
0
CRT_HSYNC_C
CRT_HSYNC
CRT_HSYNC
G
Q510
2N7002
S
D
P24
5
2A
2Y
3
4
GND
VGA _CRT_ VSYNC
R596
0
CRT_ VSYNC_C
CRT_ VSYNC
CRT_ VSYNC
External VGA Connector
AGND_CRT
U508
SN74LVC2G125
U521
North Bridge
Intel 945GM
+3VS
R270
10K
P15
U522
South Bridge
ICH7-M
CRT_ IN#
CRT_ IN#
CRT_ IN#
CRT_ IN#
L510
120Z/100M
AGND_CRT
VGA_CRT_ RED
R564
0
CRT_ RED
CRT_ RED
L4
75Z/100M
CRT_ RED
VGA_CRT_ GREEN
R590
0
CRT_ GREEN
CRT_ GREEN
L8
75Z/100M
CRT_ GREEN
VGA_CRT_BLUE
R602
0
CRT_BLUE
CRT_BLUE
L10
75Z/100M
CRT_BLUE
L515
120Z/100M
C12,C13,C14
3.3P
R31,R30,R29
75
GND
AGND_CRT
AGND_CRT

8.5 Memory Test Error-1

Extend DDR2 SO-DIMM is test error or system hangs up.


Memory Test Error
1. Check the extend SDRAM module is installed properly. (J504, J505)
2. Confirm the SDRAM socket (J504, J505) is ok, no band pins.
3. Check if on board SDRAM chips are no cold solder.
Test OK?
Yes
Correct it.
No
If your system host bus clock running at 400/533/667 MHz then make sure that SO-DIMM module meet require of PC3200/PC4200/PC5400.
Test OK?
Yes
Replace the faulty DDR2 SO-DIMM module.
No
Replace Motherboard
Board-level Troubleshooting

One of the following components or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:

U521
J504
J505
R205
R240
R250
R242
R245
R299
R304
R310

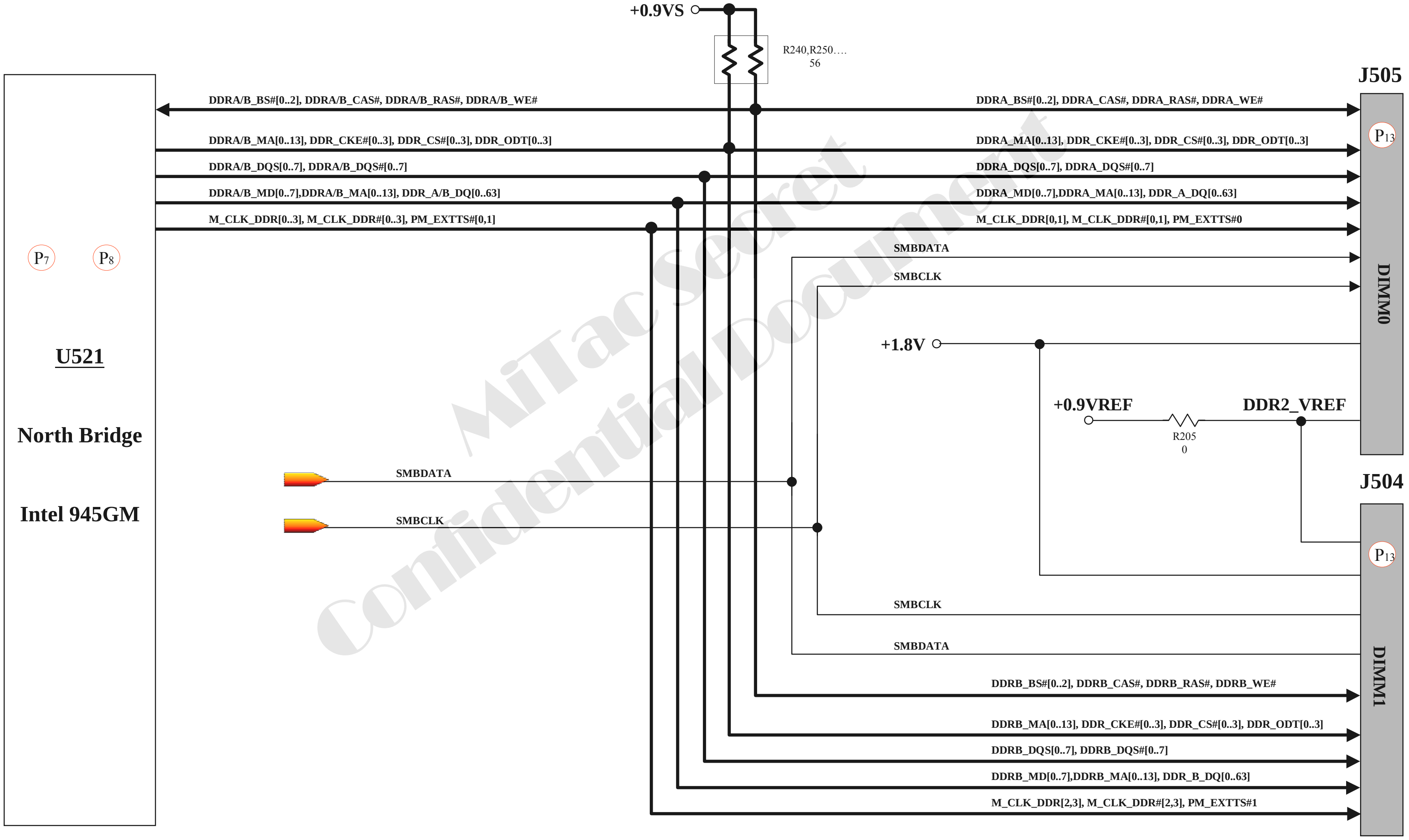
Signals:

+1.8V
+0.9VS
DDR2_VREF
DDRA/B_MA[0..13]
DDR_CKE#[0..3]
DDR_CS#[0..3]
DDR_ODT[0..3]
DDRA/B_CAS#
DDRA/B_RAS#
DDRA/B_WE#

SMBCLK
SMBDATA
M_CLK _DDR[0..3]
M_CLK _DDR#[0..3]
DDRA/B_DQS[0..7]
DDRA/B_DQS#[0..7]
DDR_A/B_DQ[0..63]
DDRA/B_MD[0..7]
DDRA/B_BS#[0..2]
PM_EXTTS#[0,1]

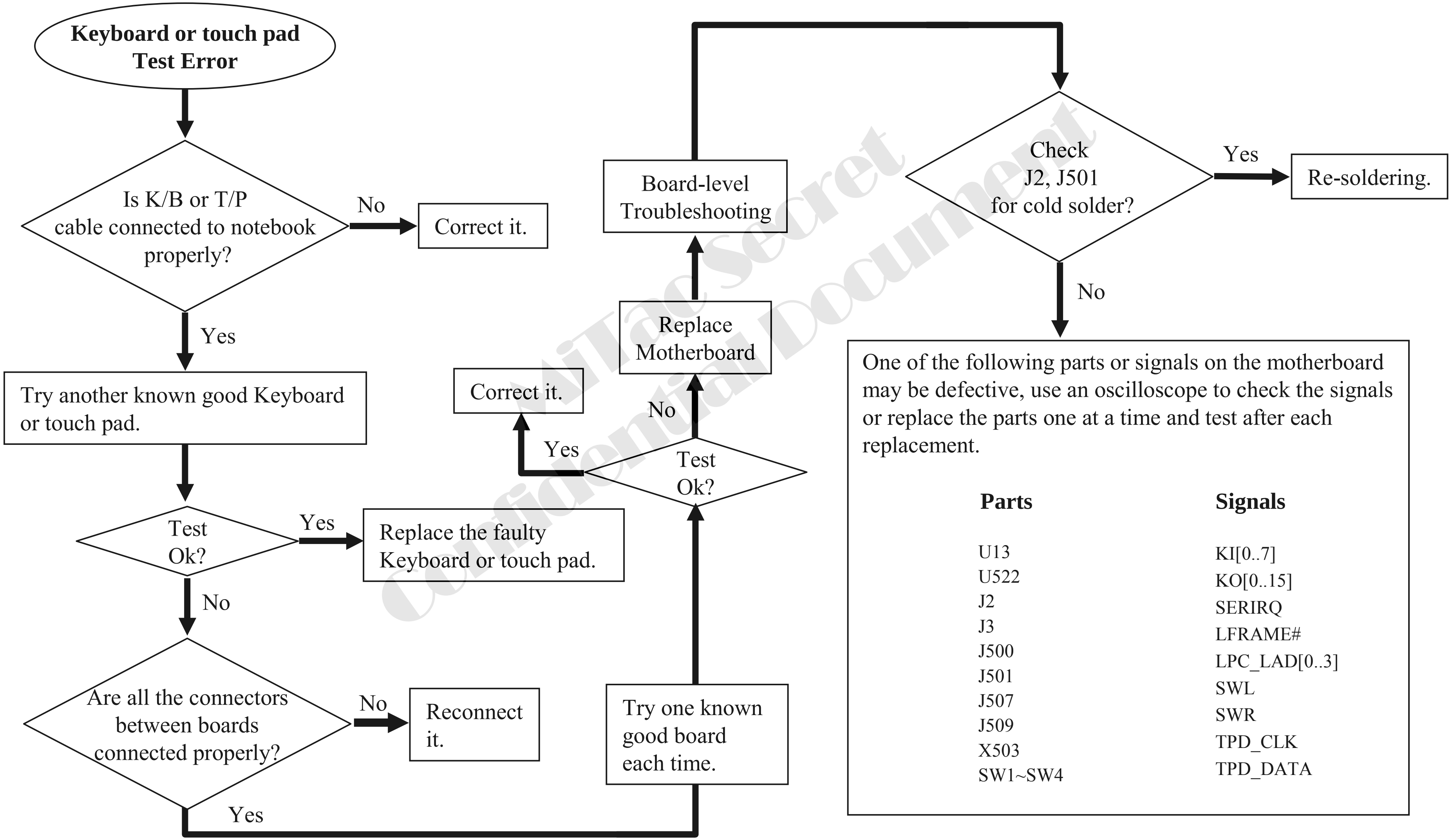
8.5 Memory Test Error-2

Extend DDR2 SO-DIMM is test error or system hangs up.


+0.9VS
R240,R250….
56
J505
DDRA/B_BS#[0..2], DDRA/B_CAS#, DDRA/B_RAS#, DDRA/B_WE#
DDRA_BS#[0..2], DDRA_CAS#, DDRA_RAS#, DDRA_WE#
DDRA/B_MA[0..13], DDR_CKE#[0..3], DDR_CS#[0..3], DDR_ODT[0..3]
DDRA_MA[0..13], DDR_CKE#[0..3], DDR_CS#[0..3], DDR_ODT[0..3]
DDRA/B_DQS[0..7], DDRA/B_DQS#[0..7]
DDRA_DQS[0..7], DDRA_DQS#[0..7]
DDRA/B_MD[0..7],DDRA/B_MA[0..13], DDR_A/B_DQ[0..63]
DDRA_MD[0..7],DDRA_MA[0..13], DDR_A_DQ[0..63]
M_CLK_DDR[0..3], M_CLK_DDR#[0..3], PM_EXTTS#[0,1]
M_CLK_DDR[0,1], M_CLK_DDR#[0,1], PM_EXTTS#0
P13
P7
P8
SMBDATA
SMBCLK
DIMM0
U521
North Bridge
Intel 945GM
+1.8V
+0.9VREF
DDR2_VREF
R205
0
J504
SMBDATA
SMBCLK
P13
SMBCLK
SMBDATA
DIMM1
DDRB_BS#[0..2], DDRB_CAS#, DDRB_RAS#, DDRB_WE#
DDRB_MA[0..13], DDR_CKE#[0..3], DDR_CS#[0..3], DDR_ODT[0..3]
DDRB_DQS[0..7], DDRB_DQS#[0..7]
DDRB_MD[0..7],DDRB_MA[0..13], DDR_B_DQ[0..63]
M_CLK_DDR[2,3], M_CLK_DDR#[2,3], PM_EXTTS#1

8.6 Keyboard (K/B) or touch pad (T/P) Test Error-1

Error message of keyboard or touch pad test error is shown or any key does not work.


Keyboard or touch pad Test Error
Is K/B or T/P cable connected to notebook properly?
No
Correct it.
Yes
Try another known good Keyboard or touch pad.
Test Ok?
Yes
Replace the faulty Keyboard or touch pad.
No
Are all the connectors between boards connected properly?
No
Reconnect it.
Yes
Try one known good board each time.
Test Ok?
Yes
Correct it.
No
Replace Motherboard
Board-level Troubleshooting
Check J2, J501 for cold solder?
Yes
Re-soldering.
No

One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts	Signals
U13	KI[0..7]
U522	KO[0..15]
J2	SERIRQ
J3	LFRAME#
J500	LPC_LAD[0..3]
J501	SWL
J507	SWR
J509	TPD_CLK
X503	TPD_DATA
SW1~SW4	

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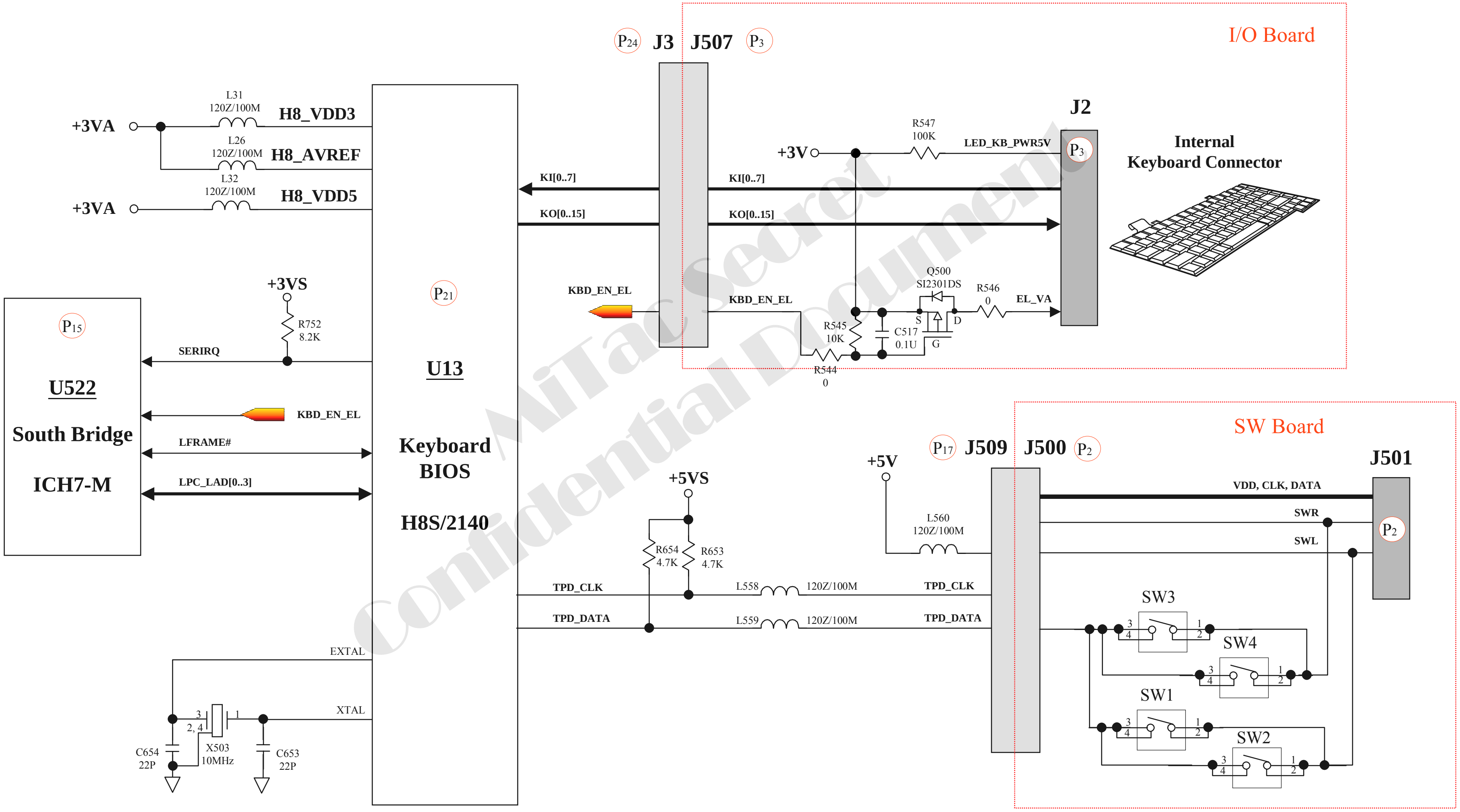
8.6 Keyboard (K/B) or touch pad (T/P) Test Error-2

Error message of keyboard or touch pad test error is shown or any key does not work.


I/O Board
P24
J3
J507
P3
J2
Internal Keyboard Connector
+3VA
L31
120Z/100M
H8_VDD3
L26
120Z/100M
H8_AVREF
L32
120Z/100M
H8_VDD5
+3VA
+3V
R547
100K
LED_KB_PWR5V
P3
KI[0..7]
KI[0..7]
KO[0..15]
KO[0..15]
+3VS
P21
P15
R752
8.2K
SERIRQ
KBD_EN_EL
KBD_EN_EL
Q500
SI2301DS
R546
0
EL_VA
S
D
G
R545
10K
C517
0.1U
R544
0
U13
U522
South Bridge
ICH7-M
KBD_EN_EL
LFRAME#
LPC_LAD[0..3]
Keyboard BIOS
H8S/2140
SW Board
P17
J509
J500
P2
J501
+5V
+5VS
VDD, CLK, DATA
SWR
SWL
P2
L560
120Z/100M
R654
4.7K
R653
4.7K
TPD_CLK
L558
120Z/100M
TPD_CLK
TPD_DATA
L559
120Z/100M
TPD_DATA
SW3
SW4
SW1
SW2
EXTAL
XTAL
C654
22P
X503
10MHz
C653
22P

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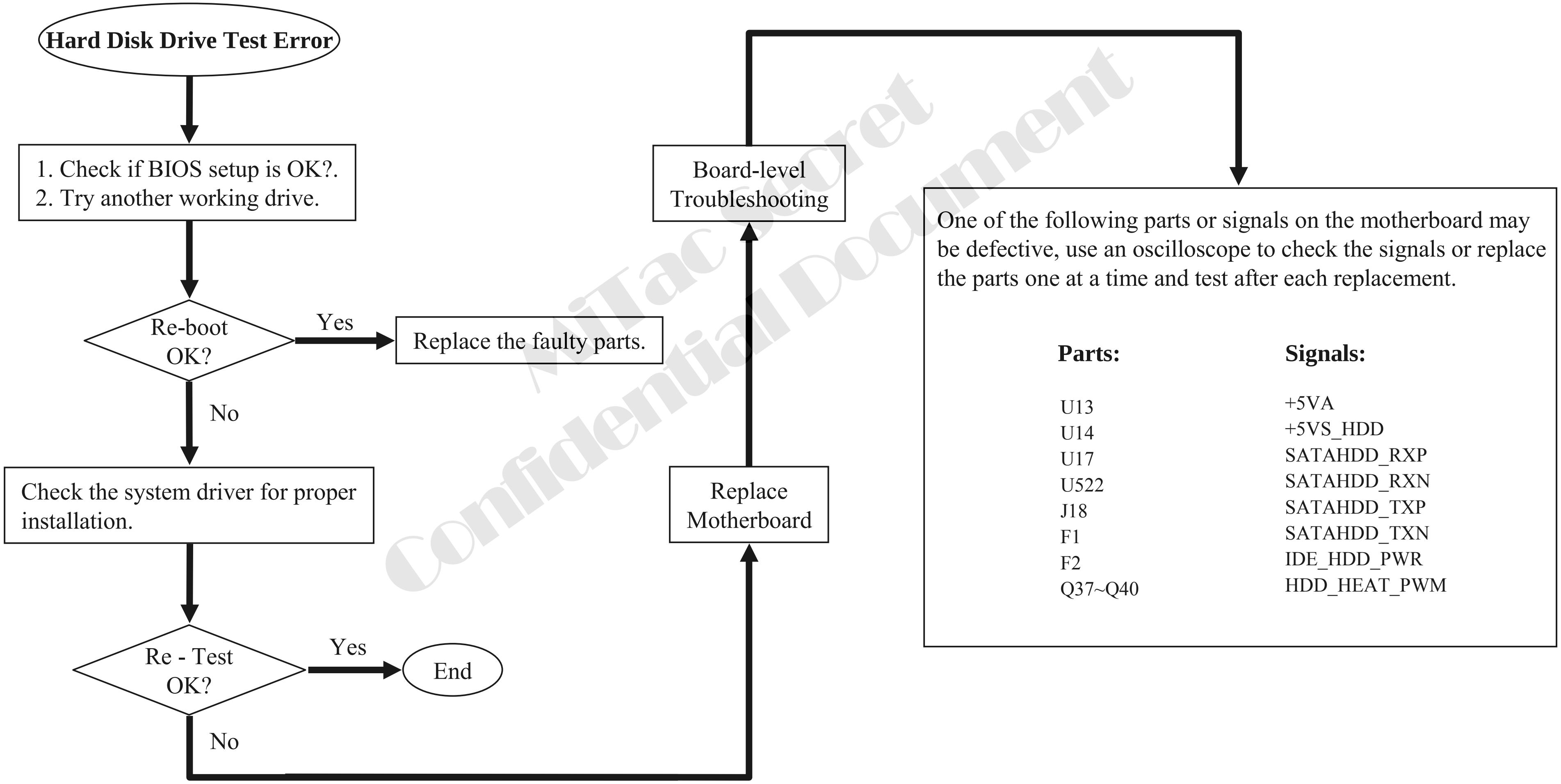
8.7 Hard Disk Drive Test Error-1

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.

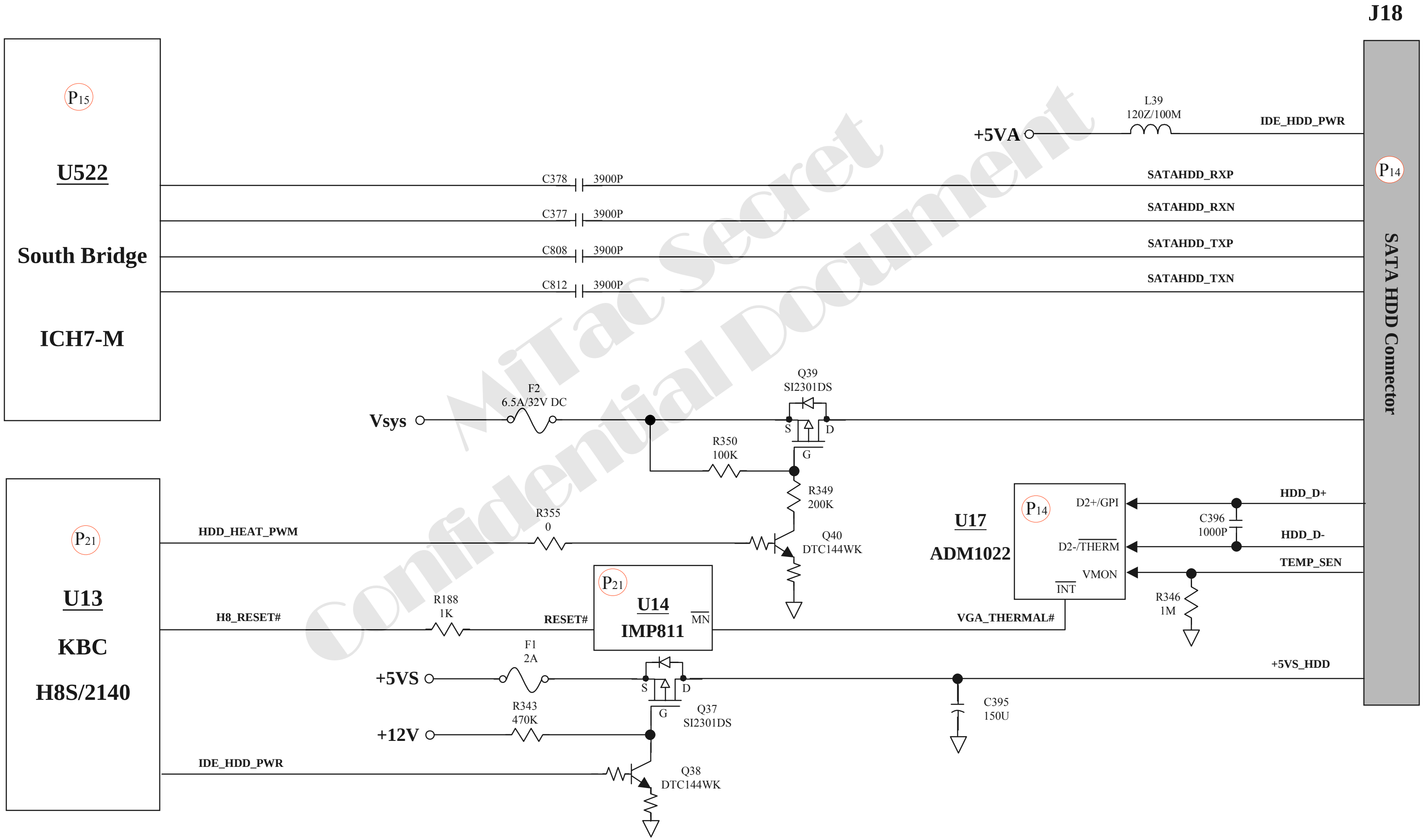

Hard Disk Drive Test Error
1. Check if BIOS setup is OK?.
2. Try another working drive.
Re-boot OK?
Yes
Replace the faulty parts.
No
Check the system driver for proper installation.
Re - Test OK?
Yes
End
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U13	+5VA
U14	+5VS_HDD
U17	SATAHDD_RXP
U522	SATAHDD_RXN
J18	SATAHDD_TXP
F1	SATAHDD_TXN
F2	IDE_HDD_PWR
Q37~Q40	HDD_HEAT_PWM

8.7 Hard Disk Drive Test Error-2

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.


J18
P15
U522
South Bridge
ICH7-M
+5VA
L39
120Z/100M
IDE_HDD_PWR
P14
C378 3900P
SATAHDD_RXP
C377 3900P
SATAHDD_RXN
C808 3900P
SATAHDD_TXP
C812 3900P
SATAHDD_TXN
SATA HDD Connector
Vsys
F2
6.5A/32V DC
Q39
SI2301DS
S
D
G
R350
100K
R349
200K
HDD_HEAT_PWM
R355
0
Q40
DTC144WK
P21
U13
KBC
H8S/2140
H8_RESET#
R188
1K
RESET#
P21
U14
IMP811
MN
U17
ADM1022
P14
D2+/GPI
D2-/THERM
VMON
INT
HDD_D+
C396
1000P
HDD_D-
TEMP_SEN
R346
1M
VGA_THERMAL#
+5VS
F1
2A
S
D
G
Q37
SI2301DS
+5VS_HDD
C395
150U
+12V
R343
470K
IDE_HDD_PWR
Q38
DTC144WK

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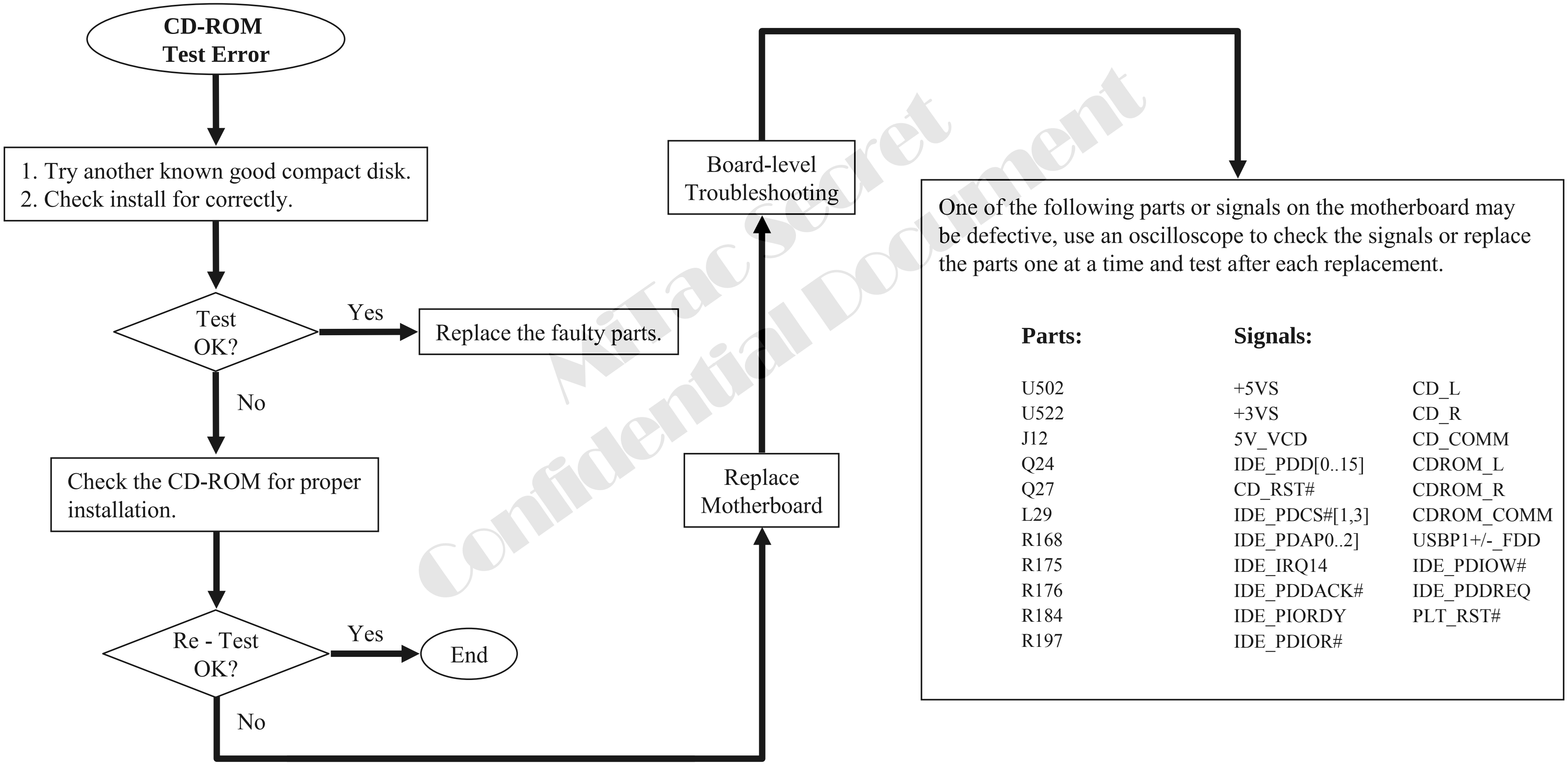
8.8 CD-ROM Test Error-1

An error message is shown when reading data from CD-ROM.


CD-ROM
Test Error
1. Try another known good compact disk.
2. Check install for correctly.
Test
OK?
Yes
Replace the faulty parts.
No
Check the CD-ROM for proper installation.
Re - Test
OK?
Yes
End
No
Replace
Motherboard
Board-level
Troubleshooting

One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**	
U502	+5VS	CD_L
U522	+3VS	CD_R
J12	5V_VCD	CD_COMM
Q24	IDE_PDD[0..15]	CDROM_L
Q27	CD_RST#	CDROM_R
L29	IDE_PDCS#[1,3]	CDROM_COMM
R168	IDE_PDAP0..2]	USBP1+/-_FDD
R175	IDE_IRQ14	IDE_PDIOW#
R176	IDE_PDDACK#	IDE_PDDREQ
R184	IDE_PIORDY	PLT_RST#
R197	IDE_PDIOR#	

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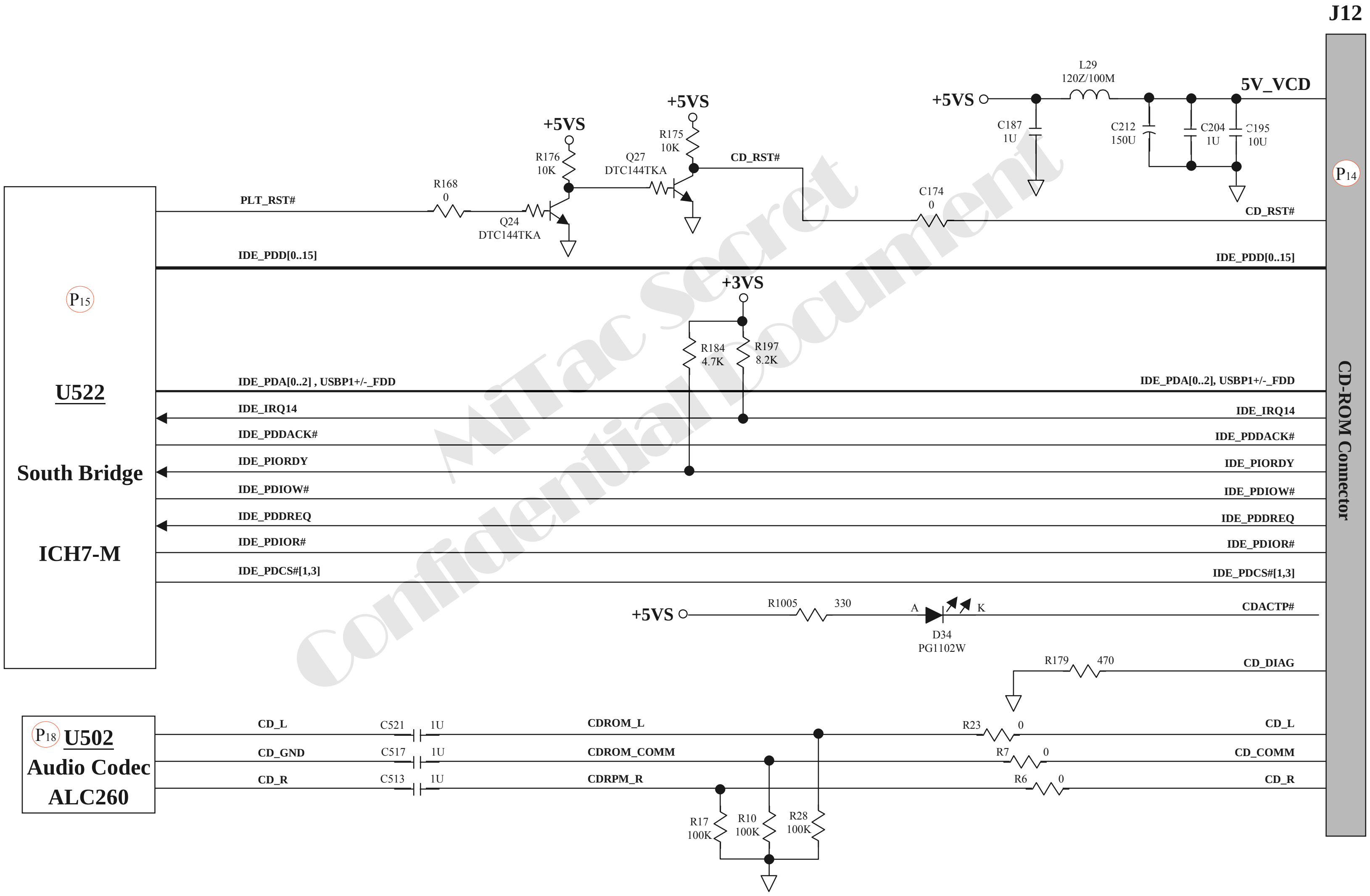
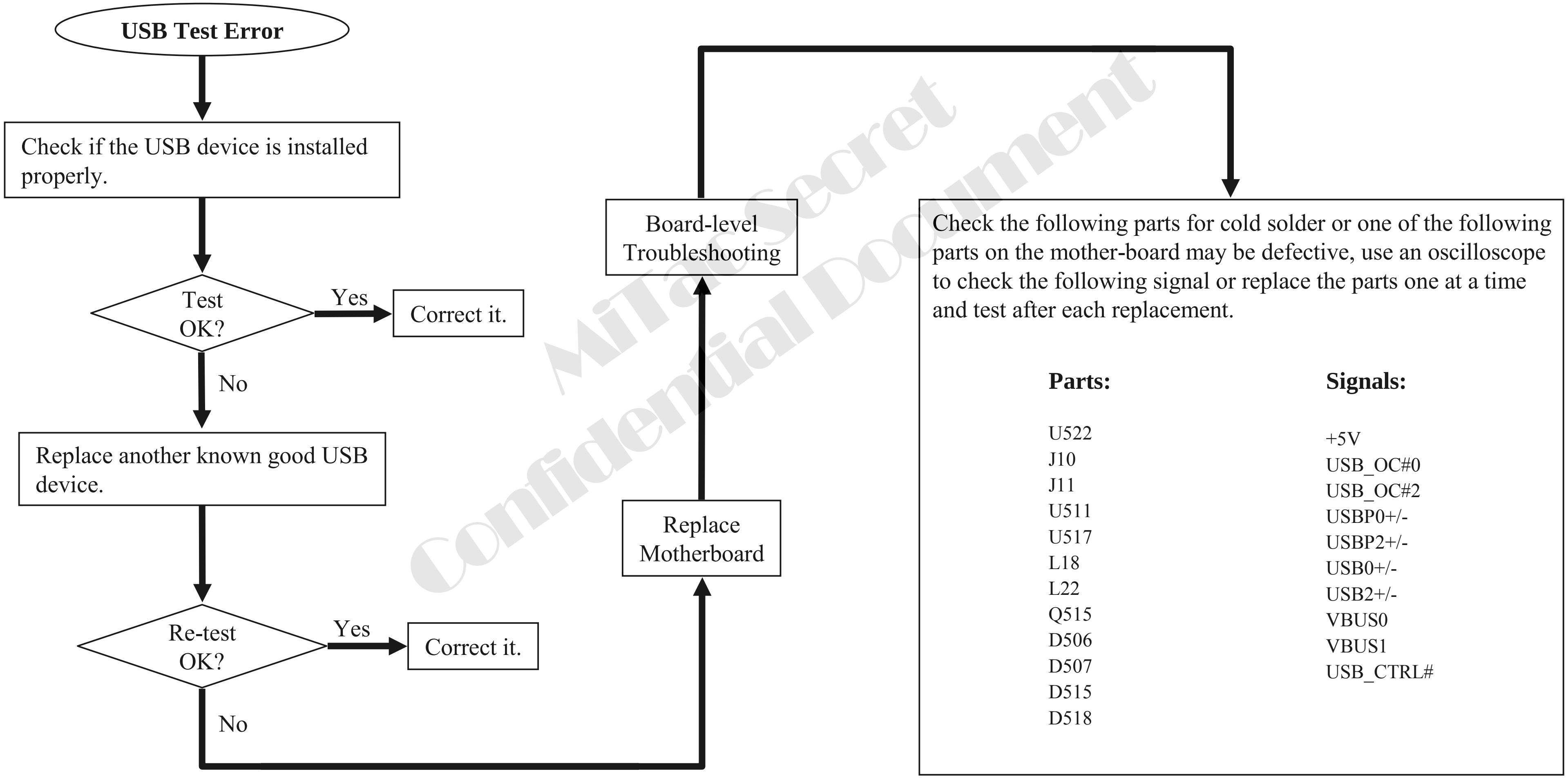
8.8 CD-ROM Test Error-2

An error message is shown when reading data from CD-ROM.


J12
L29
120Z/100M
+5VS
5V_VCD
+5VS
+5VS
R175
10K
R176
10K
Q27
DTC144TKA
CD_RST#
C187
1U
C212
150U
C204
1U
C195
10U
P14
R168
0
PLT_RST#
Q24
DTC144TKA
C174
0
CD_RST#
IDE_PDD[0..15]
IDE_PDD[0..15]
+3VS
P15
R184
4.7K
R197
8.2K
U522
South Bridge
ICH7-M
IDE_PDA[0..2] , USBP1+/-_FDD
IDE_PDA[0..2], USBP1+/-_FDD
IDE_IRQ14
IDE_IRQ14
IDE_PDDACK#
IDE_PDDACK#
IDE_PIORDY
IDE_PIORDY
IDE_PDIOW#
IDE_PDIOW#
IDE_PDDREQ
IDE_PDDREQ
IDE_PDIOR#
IDE_PDIOR#
IDE_PDCS#[1,3]
IDE_PDCS#[1,3]
CD-ROM Connector
+5VS
R1005
330
A
K
D34
PG1102W
CDACTP#
R179
470
CD_DIAG
P18
U502
Audio Codec
ALC260
CD_L
C521
1U
CDROM_L
R23
0
CD_L
CD_GND
C517
1U
CDROM_COMM
R7
0
CD_COMM
CD_R
C513
1U
CDRPM_R
R6
0
CD_R
R17
100K
R10
100K
R28
100K

8.9 USB Test Error-1

An error occurs when a USB I/O device is installed.


USB Test Error
Check if the USB device is installed properly.
Test OK?
Yes
Correct it.
No
Replace another known good USB device.
Re-test OK?
Yes
Correct it.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

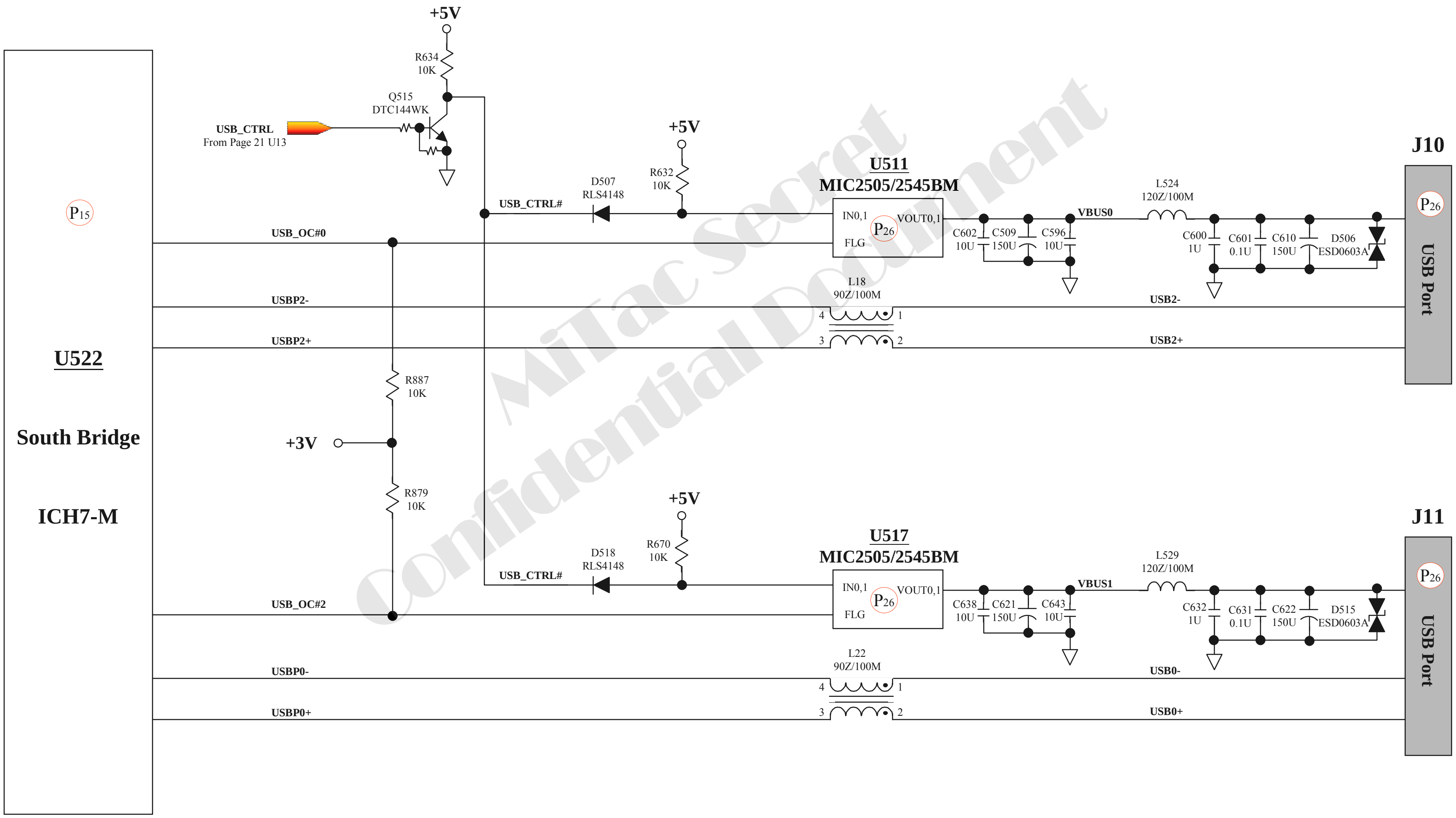
U522
J10
J11
U511
U517
L18
L22
Q515
D506
D507
D515
D518

Signals:

+5V
USB_OC#0
USB_OC#2
USBP0+/-
USBP2+/-
USB0+/-
USB2+/-
VBUS0
VBUS1
USB_CTRL#

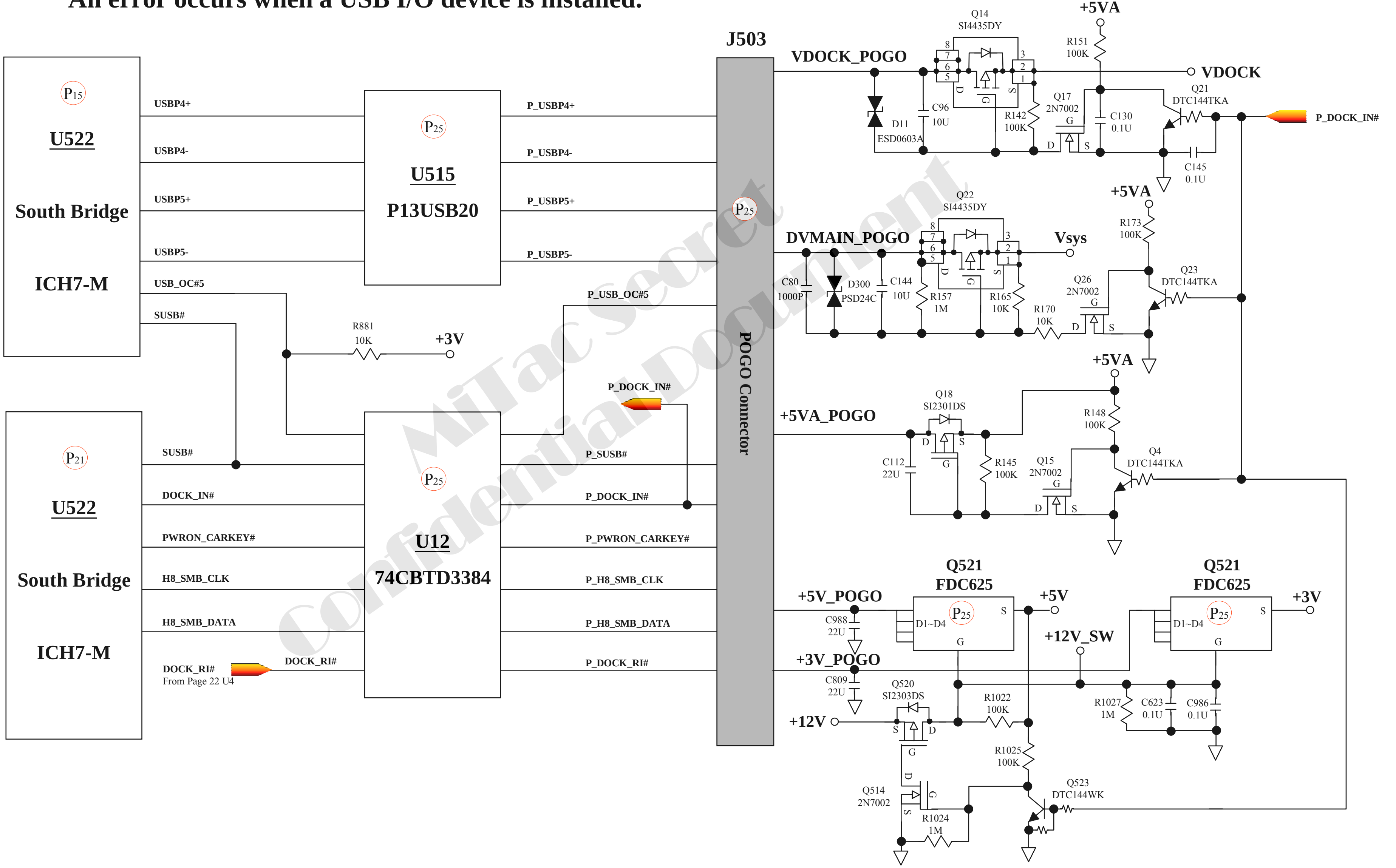
8.9 USB Test Error-2

An error occurs when a USB I/O device is installed.


+5V
R634
10K
Q515
DTC144WK
USB_CTRL
From Page 21 U13
P15
U522
South Bridge
ICH7-M
USB_OC#0
USBP2-
USBP2+
R887
10K
+3V
R879
10K
USB_OC#2
USBP0-
USBP0+
USB_CTRL#
D507
RLS4148
+5V
R632
10K
U511
MIC2505/2545BM
IN0,1
VOUT0,1
FLG
P26
C602
10U
C509
150U
C596
10U
VBUS0
L524
120Z/100M
C600
1U
C601
0.1U
C610
150U
D506
ESD0603A
L18
90Z/100M
4
1
3
2
USB2-
USB2+
J10
P26
USB Port
USB_CTRL#
D518
RLS4148
+5V
R670
10K
U517
MIC2505/2545BM
IN0,1
VOUT0,1
FLG
P26
C638
10U
C621
150U
C643
10U
VBUS1
L529
120Z/100M
C632
1U
C631
0.1U
C622
150U
D515
ESD0603A
L22
90Z/100M
4
1
3
2
USB0-
USB0+
J11
P26
USB Port

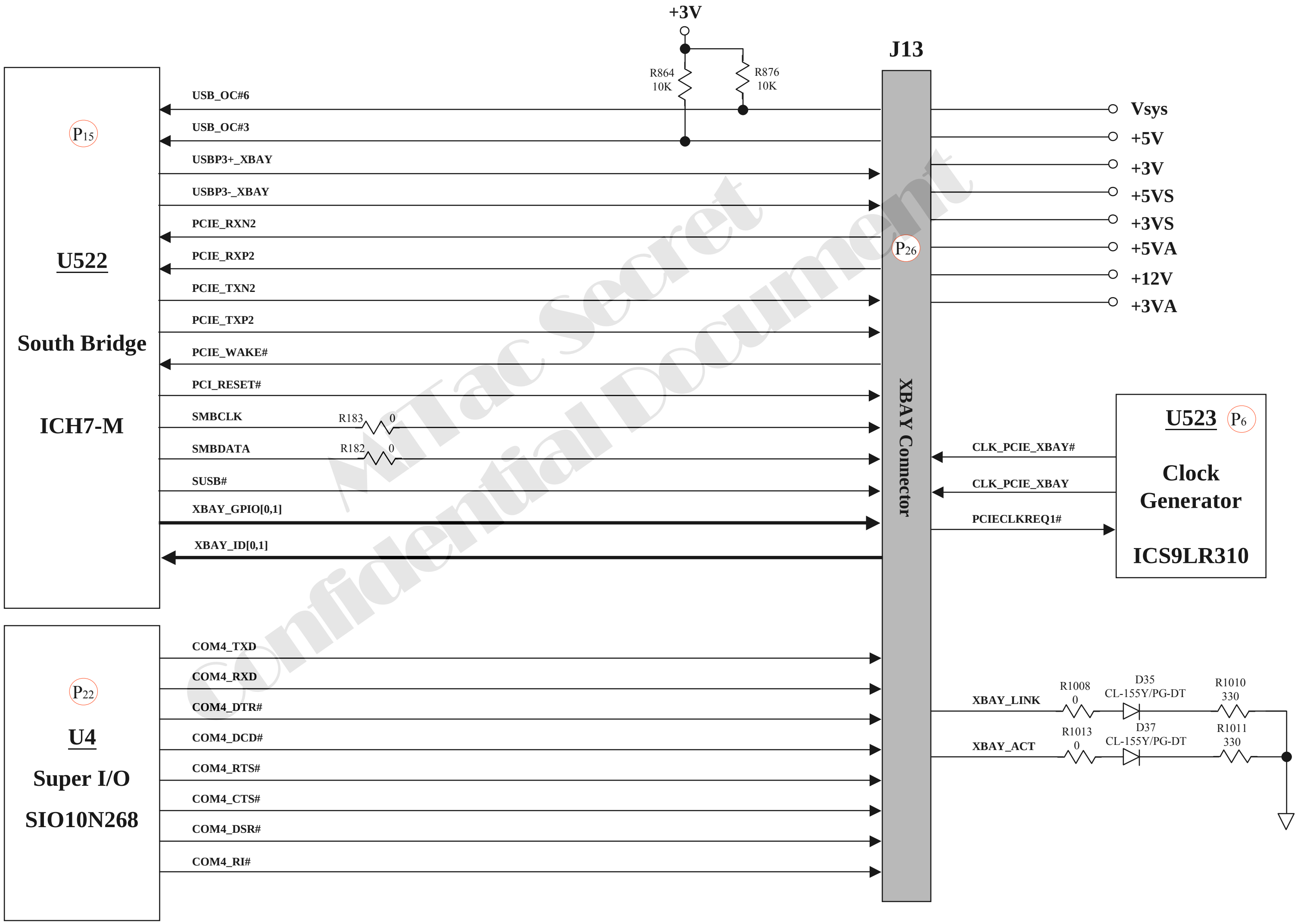
8.9 USB Test Error-3 (POGO)

An error occurs when a USB I/O device is installed.


J503
U522
South Bridge
ICH7-M
P15
P21
P25
U515
P13USB20
U12
74CBTD3384
POGO Connector
USBP4+
USBP4-
USBP5+
USBP5-
USB_OC#5
SUSB#
P_USBP4+
P_USBP4-
P_USBP5+
P_USBP5-
P_USB_OC#5
R881
10K
+3V
P_DOCK_IN#
DOCK_IN#
PWRON_CARKEY#
H8_SMB_CLK
H8_SMB_DATA
DOCK_RI#
From Page 22 U4
P_SUSB#
P_PWRON_CARKEY#
P_H8_SMB_CLK
P_H8_SMB_DATA
P_DOCK_RI#
VDOCK_POGO
Q14
SI4435DY
+5VA
R151
100K
VDOCK
D11
ESD0603A
C96
10U
R142
100K
Q17
2N7002
C130
0.1U
Q21
DTC144TKA
C145
0.1U
DVMAIN_POGO
Q22
SI4435DY
Vsys
R173
100K
C80
1000P
D300
PSD24C
C144
10U
R157
1M
R165
10K
R170
10K
Q26
2N7002
Q23
DTC144TKA
+5VA_POGO
Q18
SI2301DS
R148
100K
C112
22U
R145
100K
Q15
2N7002
Q4
DTC144TKA
Q521
FDC625
+5V_POGO
C988
22U
D1~D4
+5V
+12V_SW
+3V_POGO
C809
22U
Q520
SI2303DS
R1022
100K
R1027
1M
C623
0.1U
C986
0.1U
+12V
R1025
100K
Q514
2N7002
R1024
1M
Q523
DTC144WK

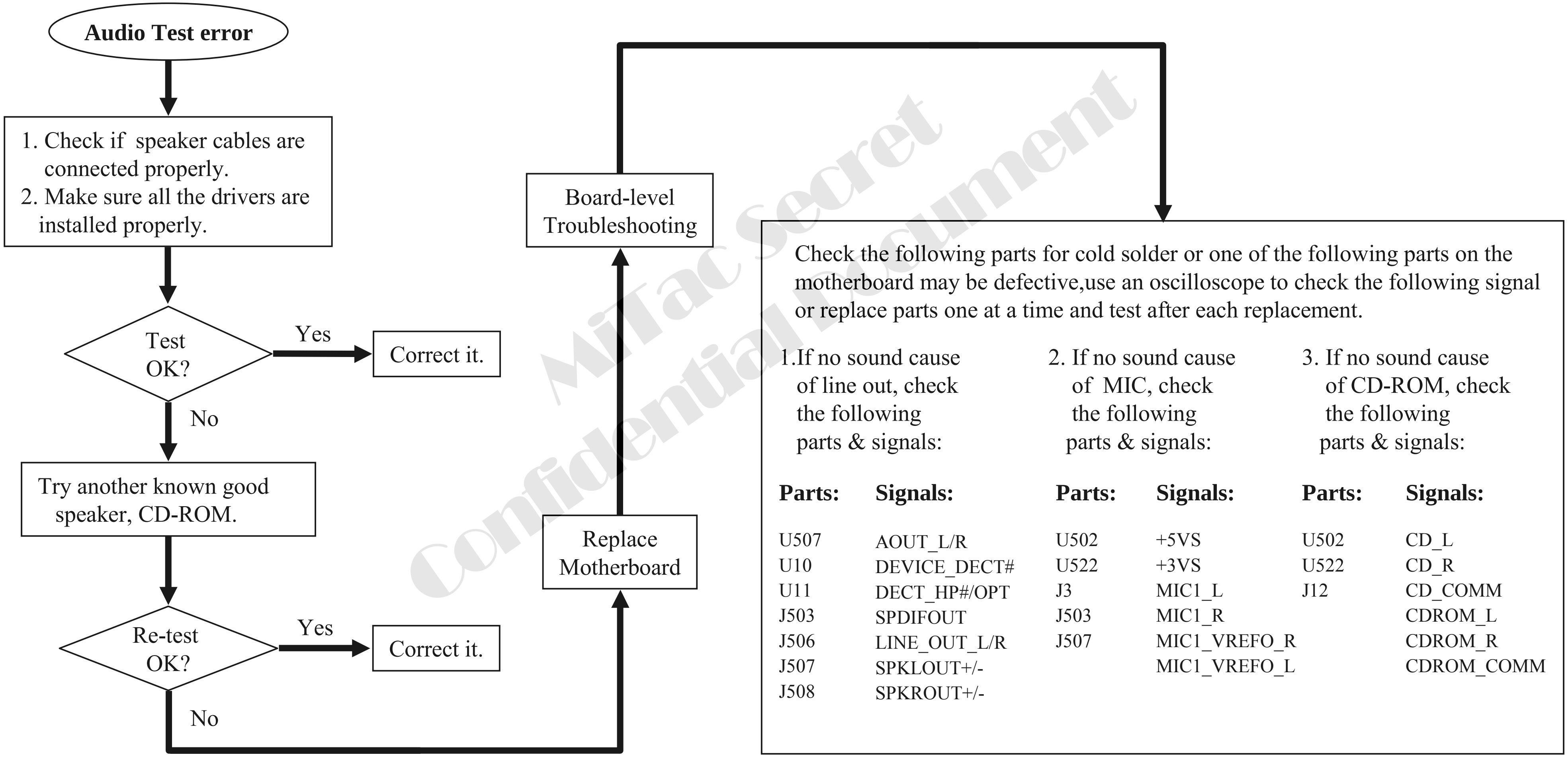
8.9 USB Test Error-4 (X-BAY)

An error occurs when a USB I/O device is installed.


+3V
R864
10K
R876
10K
J13
P15
U522
South Bridge
ICH7-M
USB_OC#6
USB_OC#3
USBP3+_XBAY
USBP3-_XBAY
PCIE_RXN2
PCIE_RXP2
PCIE_TXN2
PCIE_TXP2
PCIE_WAKE#
PCI_RESET#
SMBCLK
R183
0
SMBDATA
R182
0
SUSB#
XBAY_GPIO[0,1]
XBAY_ID[0,1]
P26
XBAY Connector
Vsys
+5V
+3V
+5VS
+3VS
+5VA
+12V
+3VA
U523
P6
Clock
Generator
ICS9LR310
CLK_PCIE_XBAY#
CLK_PCIE_XBAY
PCIECLKREQ1#
P22
U4
Super I/O
SIO10N268
COM4_TXD
COM4_RXD
COM4_DTR#
COM4_DCD#
COM4_RTS#
COM4_CTS#
COM4_DSR#
COM4_RI#
XBAY_LINK
R1008
0
D35
CL-155Y/PG-DT
R1010
330
XBAY_ACT
R1013
0
D37
CL-155Y/PG-DT
R1011
330

8.10 Audio Test Error-1

No sound from speaker after audio driver is installed.


Audio Test error
1. Check if speaker cables are connected properly.
2. Make sure all the drivers are installed properly.
Test OK?
Yes
Correct it.
No
Try another known good speaker, CD-ROM.
Re-test OK?
Yes
Correct it.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	**Signals:**
U507	AOUT_L/R
U10	DEVICE_DECT#
U11	DECT_HP#/OPT
J503	SPDIFOUT
J506	LINE_OUT_L/R
J507	SPKLOUT+/-
J508	SPKROUT+/-

2. If no sound cause of MIC, check the following parts & signals:

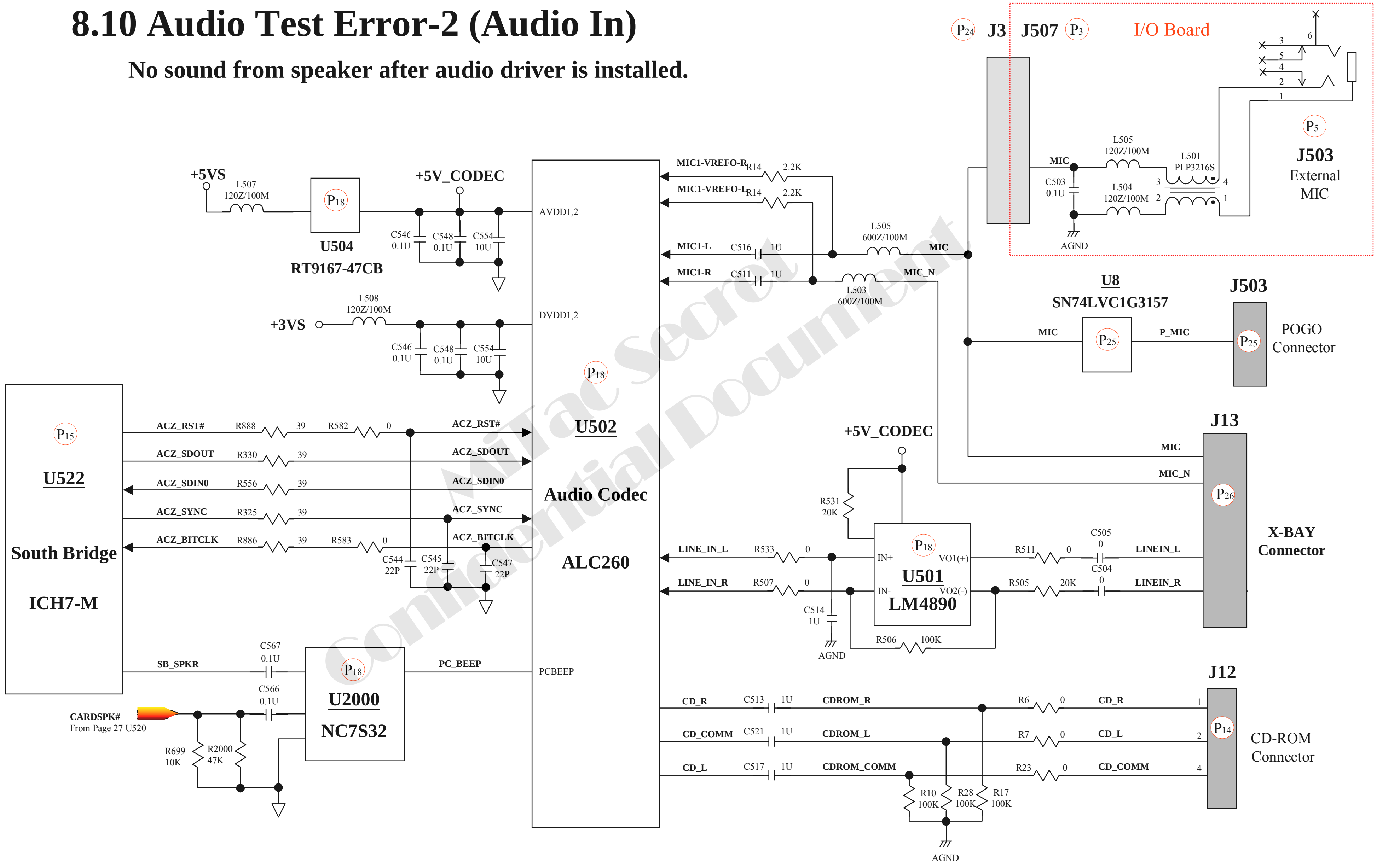
Parts:	**Signals:**
U502	+5VS
U522	+3VS
J3	MIC1_L
J503	MIC1_R
J507	MIC1_VREFO_R
	MIC1_VREFO_L

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	**Signals:**
U502	CD_L
U522	CD_R
J12	CD_COMM
	CDROM_L
	CDROM_R
	CDROM_COMM

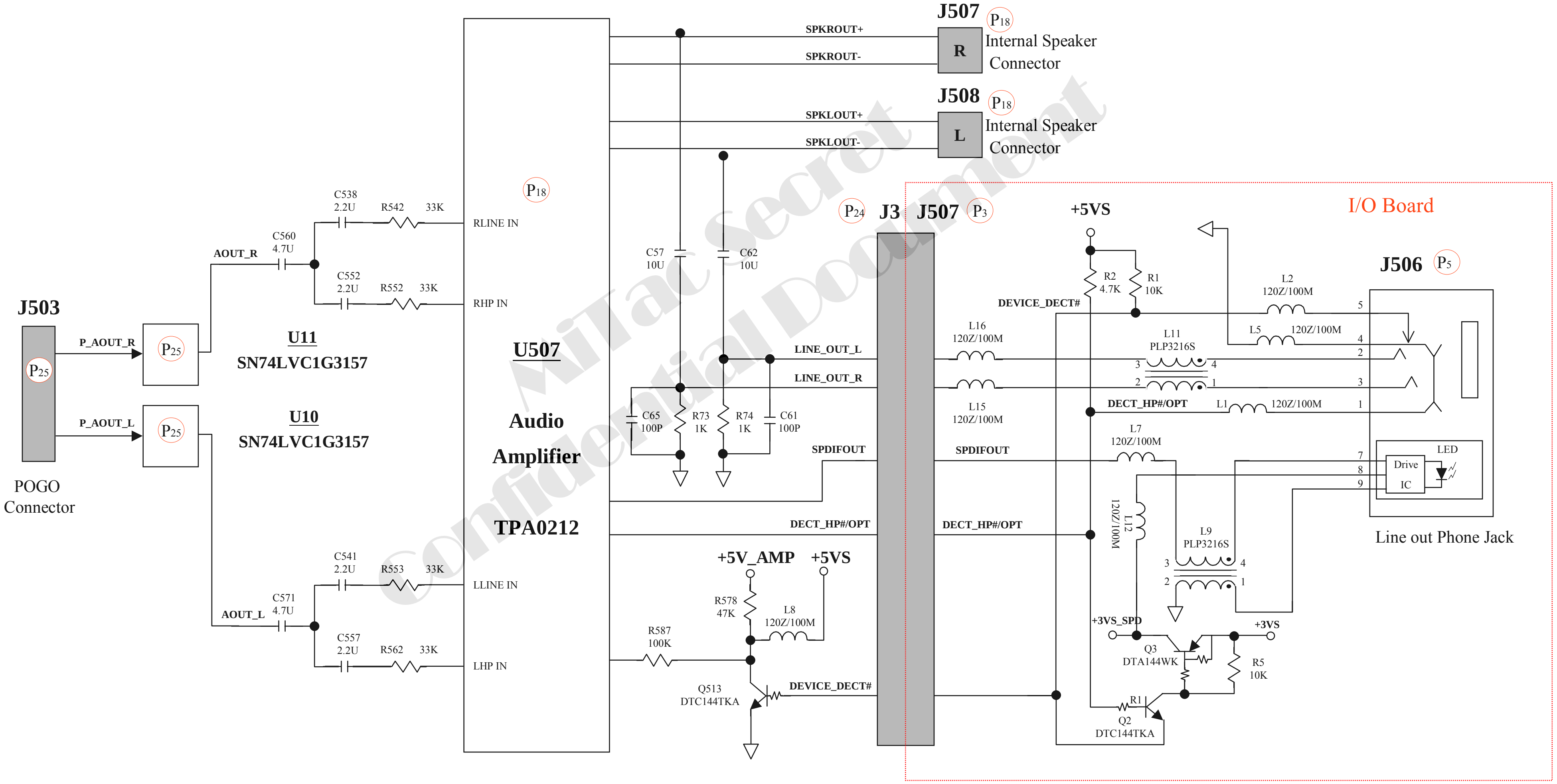
8.10 Audio Test Error-2 (Audio In)

No sound from speaker after audio driver is installed.


P24
J3
J507
P3
I/O Board
3
6
5
4
2
1
P5
J503
External
MIC
MIC
L505
120Z/100M
L501
PLP3216S
C503
0.1U
L504
120Z/100M
AGND
+5VS
L507
120Z/100M
P18
U504
RT9167-47CB
+5V_CODEC
C546
0.1U
C548
0.1U
C554
10U
AVDD1,2
MIC1-VREFO-R
R14
2.2K
MIC1-VREFO-L
R14
2.2K
MIC1-L
C516
1U
L505
600Z/100M
MIC
MIC1-R
C511
1U
L503
600Z/100M
MIC_N
+3VS
L508
120Z/100M
C546
0.1U
C548
0.1U
C554
10U
DVDD1,2
U8
SN74LVC1G3157
MIC
P25
P_MIC
J503
P25
POGO
Connector
P15
U522
South Bridge
ICH7-M
ACZ_RST#
R888
39
R582
0
ACZ_RST#
ACZ_SDOUT
R330
39
ACZ_SDOUT
ACZ_SDIN0
R556
39
ACZ_SDIN0
ACZ_SYNC
R325
39
ACZ_SYNC
ACZ_BITCLK
R886
39
R583
0
ACZ_BITCLK
C544
22P
C545
22P
C547
22P
P18
U502
Audio Codec
ALC260
+5V_CODEC
J13
MIC
MIC_N
P26
X-BAY
Connector
R531
20K
P18
U501
LM4890
IN+
IN-
VO1(+)
VO2(-)
LINE_IN_L
R533
0
LINE_IN_R
R507
0
C514
1U
AGND
R506
100K
R511
0
C505
0
LINEIN_L
R505
20K
C504
0
LINEIN_R
SB_SPKR
C567
0.1U
C566
0.1U
P18
U2000
NC7S32
PC_BEEP
PCBEEP
CARDSPK#
From Page 27 U520
R699
10K
R2000
47K
J12
CD_R
C513
1U
CDROM_R
R6
0
CD_R
1
CD_COMM
C521
1U
CDROM_L
R7
0
CD_L
2
P14
CD-ROM
Connector
CD_L
C517
1U
CDROM_COMM
R23
0
CD_COMM
4
R10
100K
R28
100K
R17
100K
AGND

8.10 Audio Test Error-3 (Audio Out)

No sound from speaker after audio driver is installed.


J507 P18
SPKROUT+
SPKROUT-
R
Internal Speaker Connector
J508 P18
SPKLOUT+
SPKLOUT-
L
Internal Speaker Connector
P18
C538 2.2U
R542 33K
RLINE IN
C560 4.7U
AOUT_R
C552 2.2U
R552 33K
RHP IN
J503
P_AOUT_R
P25
P25
U11
SN74LVC1G3157
U507
Audio Amplifier
TPA0212
P_AOUT_L
P25
U10
SN74LVC1G3157
POGO Connector
C541 2.2U
R553 33K
LLINE IN
C571 4.7U
AOUT_L
C557 2.2U
R562 33K
LHP IN
C57 10U
C62 10U
C65 100P
R73 1K
R74 1K
C61 100P
LINE_OUT_L
LINE_OUT_R
SPDIFOUT
DECT_HP#/OPT
+5V_AMP
+5VS
R578 47K
L8 120Z/100M
R587 100K
Q513 DTC144TKA
DEVICE_DECT#
P24
J3
J507
P3
+5VS
I/O Board
R2 4.7K
R1 10K
DEVICE_DECT#
L2 120Z/100M
J506 P5
L16 120Z/100M
L11 PLP3216S
L5 120Z/100M
L15 120Z/100M
DECT_HP#/OPT
L1 120Z/100M
L7 120Z/100M
SPDIFOUT
LED
Drive IC
L12 120Z/100M
L9 PLP3216S
DECT_HP#/OPT
Line out Phone Jack
+3VS_SPD
+3VS
Q3 DTA144WK
R5 10K
R1
Q2 DTC144TKA
1
2
3
4
5
7
8
9

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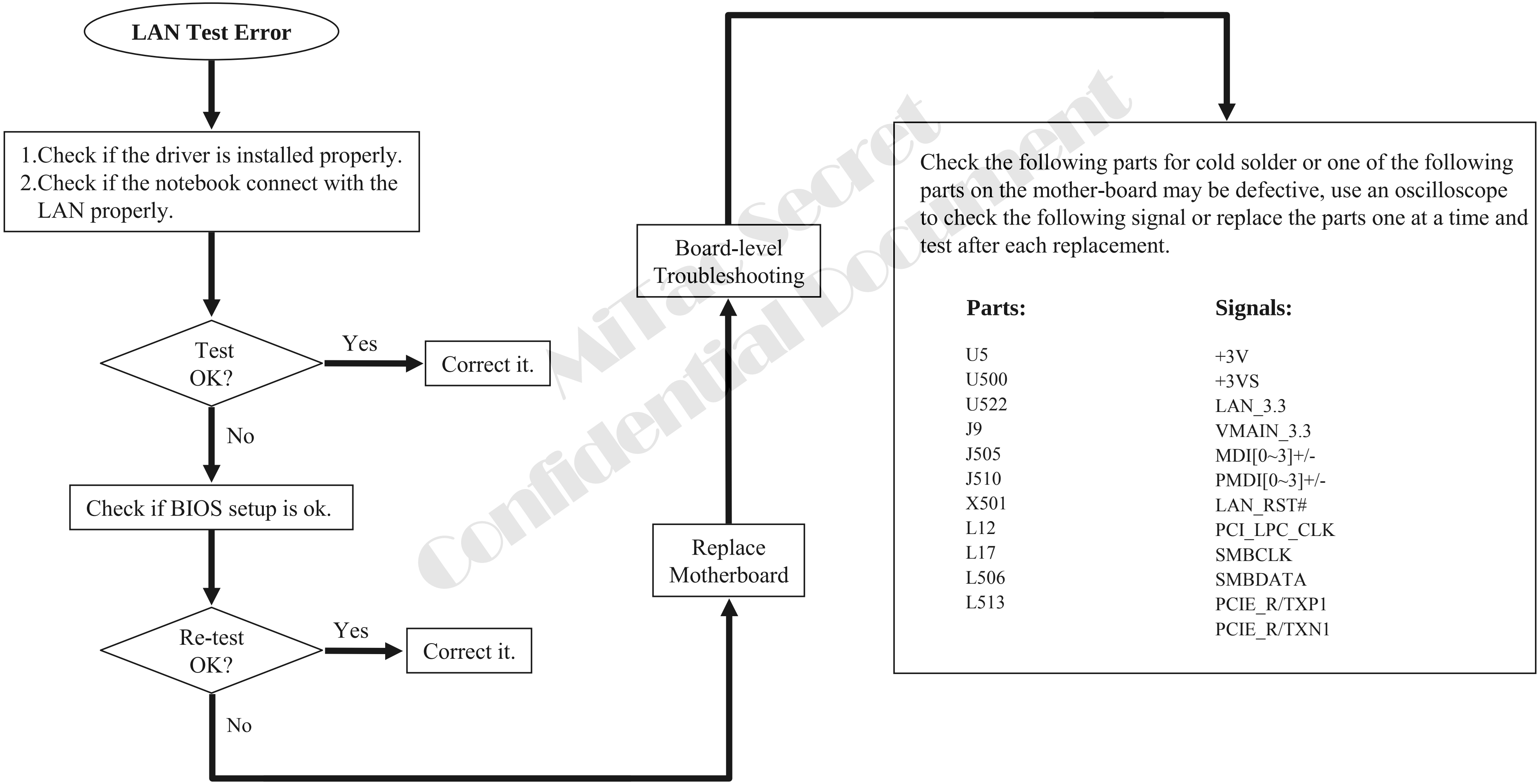
8.11 LAN Test Error-1

An error occurs when a LAN device is installed.


LAN Test Error
1.Check if the driver is installed properly.
2.Check if the notebook connect with the LAN properly.
Test OK?
Yes
Correct it.
No
Check if BIOS setup is ok.
Re-test OK?
Yes
Correct it.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U5
U500
U522
J9
J505
J510
X501
L12
L17
L506
L513

Signals:

+3V
+3VS
LAN_3.3
VMAIN_3.3
MDI[0~3]+/-
PMDI[0~3]+/-
LAN_RST#
PCI_LPC_CLK
SMBCLK
SMBDATA
PCIE_R/TXP1
PCIE_R/TXN1

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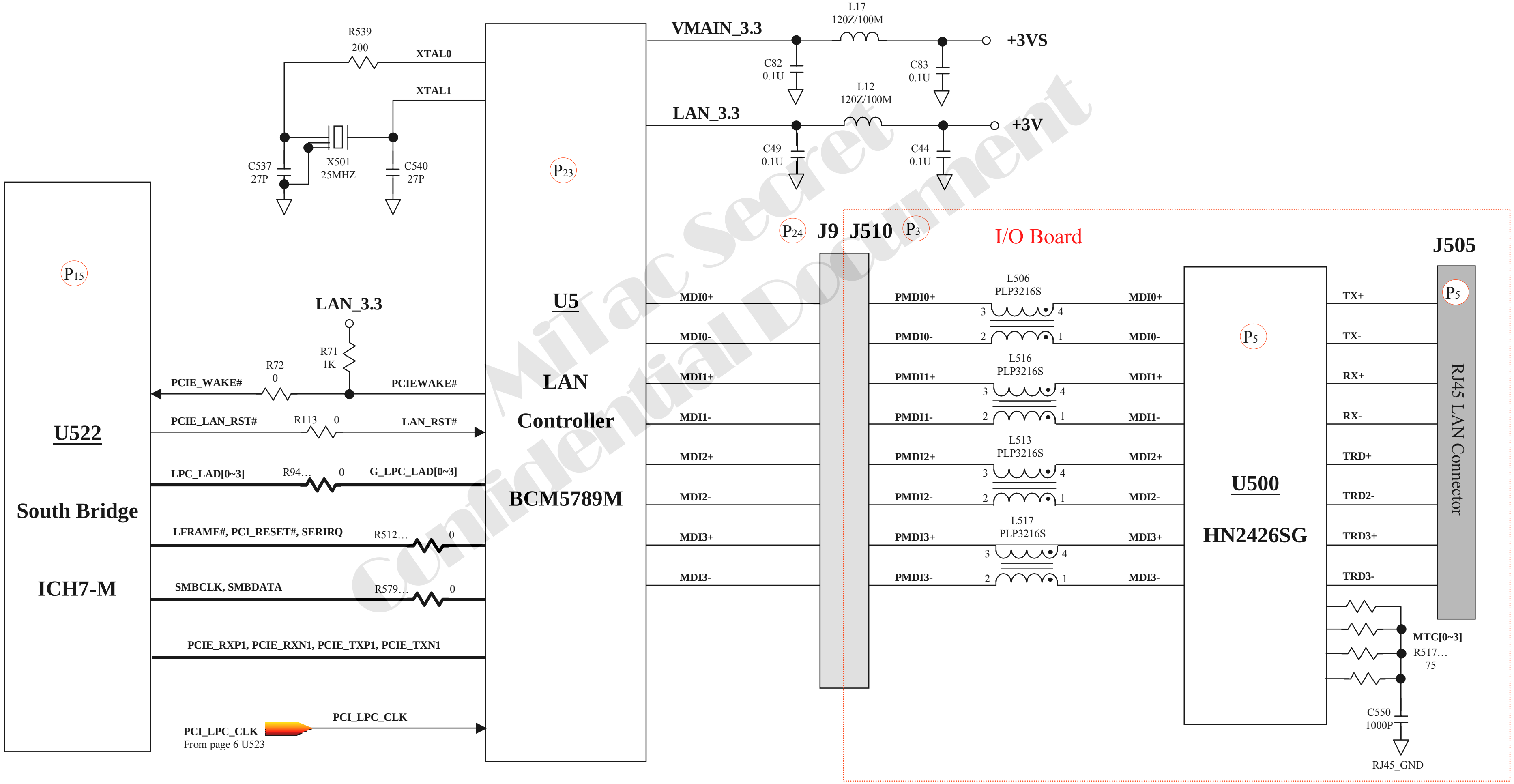
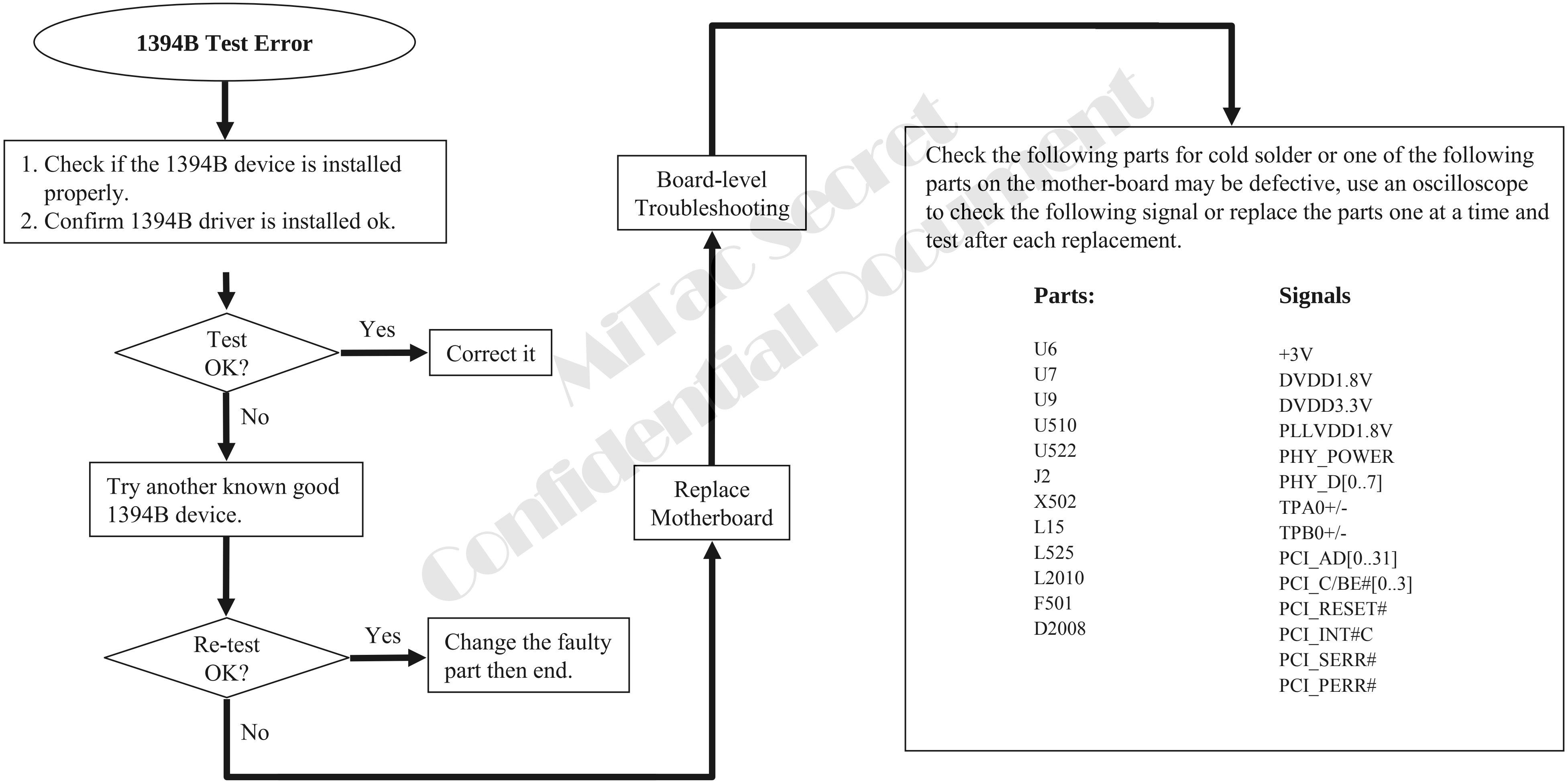
8.11 LAN Test Error-2

An error occurs when a LAN device is installed.


R539
200
XTAL0
XTAL1
C537
27P
X501
25MHZ
C540
27P
VMAIN_3.3
L17
120Z/100M
+3VS
C82
0.1U
C83
0.1U
LAN_3.3
L12
120Z/100M
+3V
C49
0.1U
C44
0.1U
P23
P15
U522
South Bridge
ICH7-M
LAN_3.3
R71
1K
R72
0
PCIE_WAKE#
PCIEWAKE#
PCIE_LAN_RST#
R113
0
LAN_RST#
LPC_LAD[0~3]
R94…
0
G_LPC_LAD[0~3]
LFRAME#, PCI_RESET#, SERIRQ
R512…
0
SMBCLK, SMBDATA
R579…
0
PCIE_RXP1, PCIE_RXN1, PCIE_TXP1, PCIE_TXN1
PCI_LPC_CLK
PCI_LPC_CLK
From page 6 U523
U5
LAN
Controller
BCM5789M
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
P24
J9
J510
P3
I/O Board
PMDI0+
PMDI0-
PMDI1+
PMDI1-
PMDI2+
PMDI2-
PMDI3+
PMDI3-
L506
PLP3216S
L516
PLP3216S
L513
PLP3216S
L517
PLP3216S
3
4
2
1
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
P5
U500
HN2426SG
TX+
TX-
RX+
RX-
TRD+
TRD2-
TRD3+
TRD3-
J505
P5
RJ45 LAN Connector
MTC[0~3]
R517…
75
C550
1000P
RJ45_GND

8.12 1394B Test Error-1

An error occurs when a 1394 device is installed.


1394B Test Error
1. Check if the 1394B device is installed properly.
2. Confirm 1394B driver is installed ok.
Test OK?
Yes
Correct it
No
Try another known good 1394B device.
Re-test OK?
Yes
Change the faulty part then end.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U6
U7
U9
U510
U522
J2
X502
L15
L525
L2010
F501
D2008

Signals

+3V
DVDD1.8V
DVDD3.3V
PLLVDD1.8V
PHY_POWER
PHY_D[0..7]
TPA0+/-
TPB0+/-
PCI_AD[0..31]
PCI_C/BE#[0..3]
PCI_RESET#
PCI_INT#C
PCI_SERR#
PCI_PERR#

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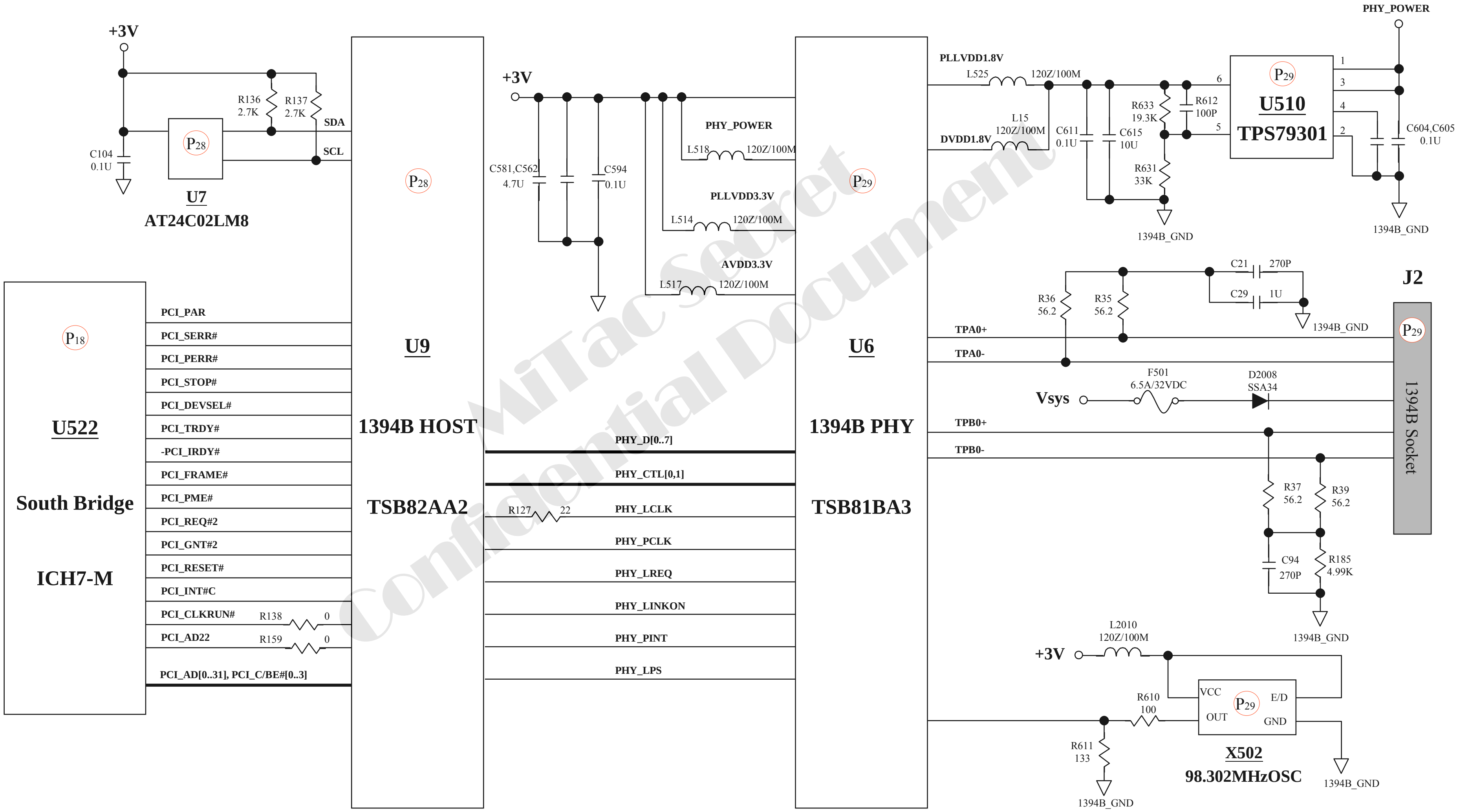
8.12 1394B Test Error-2

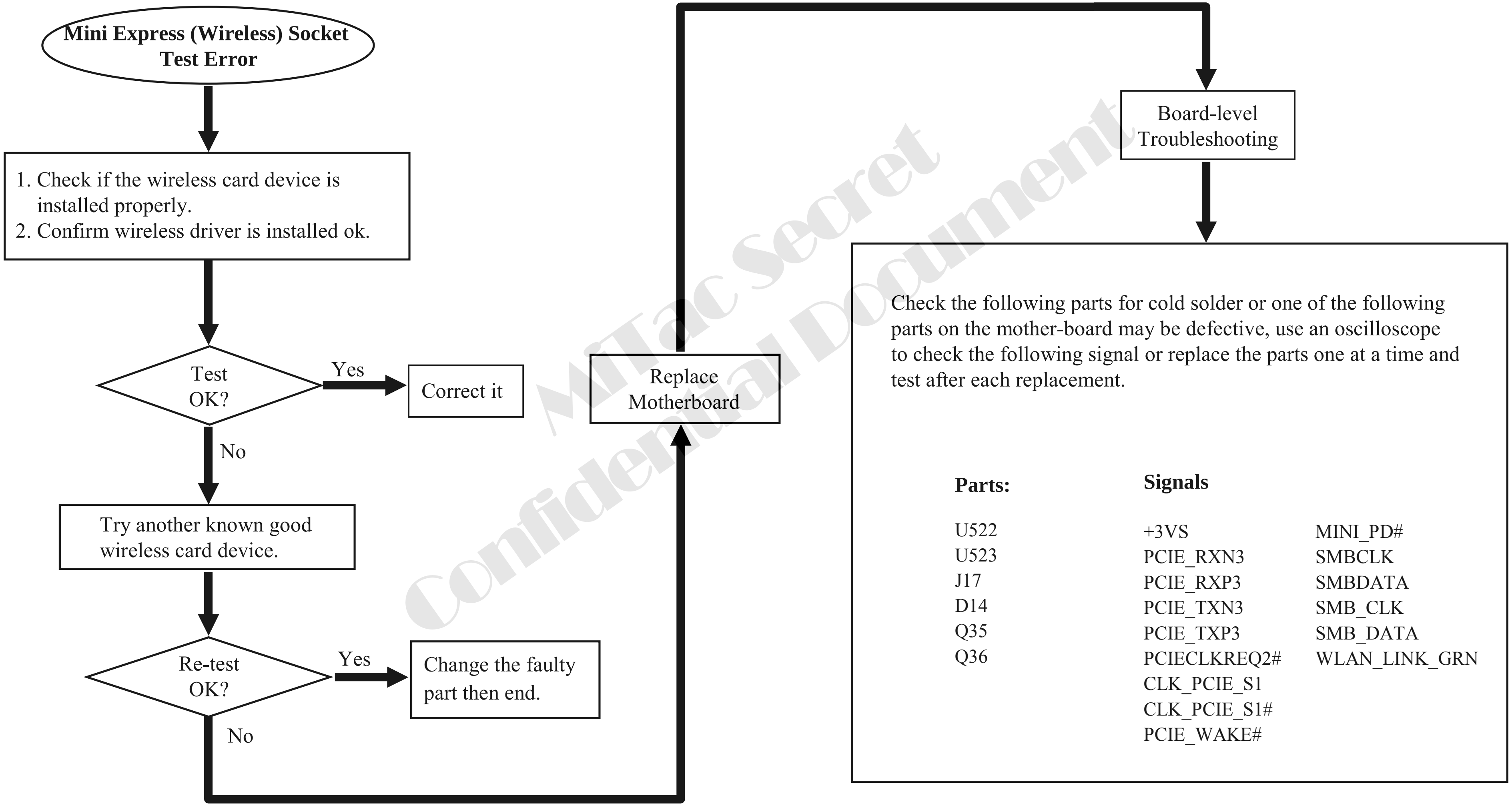
An error occurs when a 1394 device is installed.



+3V
R136
2.7K
R137
2.7K
SDA
SCL
C104
0.1U
P28
U7
AT24C02LM8
P18
U522
South Bridge
ICH7-M
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
-PCI_IRDY#
PCI_FRAME#
PCI_PME#
PCI_REQ#2
PCI_GNT#2
PCI_RESET#
PCI_INT#C
PCI_CLKRUN#
R138
0
PCI_AD22
R159
0
PCI_AD[0..31], PCI_C/BE#[0..3]
P28
U9
1394B HOST
TSB82AA2
+3V
C581,C562
4.7U
C594
0.1U
PHY_POWER
L518
120Z/100M
PLLVDD3.3V
L514
120Z/100M
AVDD3.3V
L517
120Z/100M
PHY_D[0..7]
PHY_CTL[0,1]
R127
22
PHY_LCLK
PHY_PCLK
PHY_LREQ
PHY_LINKON
PHY_PINT
PHY_LPS
P29
U6
1394B PHY
TSB81BA3
PLLVDD1.8V
L525
120Z/100M
L15
120Z/100M
DVDD1.8V
C611
0.1U
C615
10U
R633
19.3K
R612
100P
R631
33K
1394B_GND
PHY_POWER
6
5
1
3
4
2
P29
U510
TPS79301
C604,C605
0.1U
1394B_GND
C21
270P
C29
1U
R36
56.2
R35
56.2
1394B_GND
J2
P29
1394B Socket
TPA0+
TPA0-
Vsys
F501
6.5A/32VDC
D2008
SSA34
TPB0+
TPB0-
R37
56.2
R39
56.2
C94
270P
R185
4.99K
1394B_GND
+3V
L2010
120Z/100M
R610
100
VCC
OUT
E/D
GND
P29
X502
98.302MHzOSC
R611
133
1394B_GND
1394B_GND

8.13 Mini Express (Wireless) Socket Test Error-1

An error occurs when a wireless card device is installed.


Mini Express (Wireless) Socket Test Error
1. Check if the wireless card device is installed properly.
2. Confirm wireless driver is installed ok.
Test OK?
Yes
Correct it
No
Try another known good wireless card device.
Re-test OK?
Yes
Change the faulty part then end.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U522
U523
J17
D14
Q35
Q36

Signals

+3VS
PCIE_RXN3
PCIE_RXP3
PCIE_TXN3
PCIE_TXP3
PCIECLKREQ2#
CLK_PCIE_S1
CLK_PCIE_S1#
PCIE_WAKE#

MINI_PD#
SMBCLK
SMBDATA
SMB_CLK
SMB_DATA
WLAN_LINK_GRN

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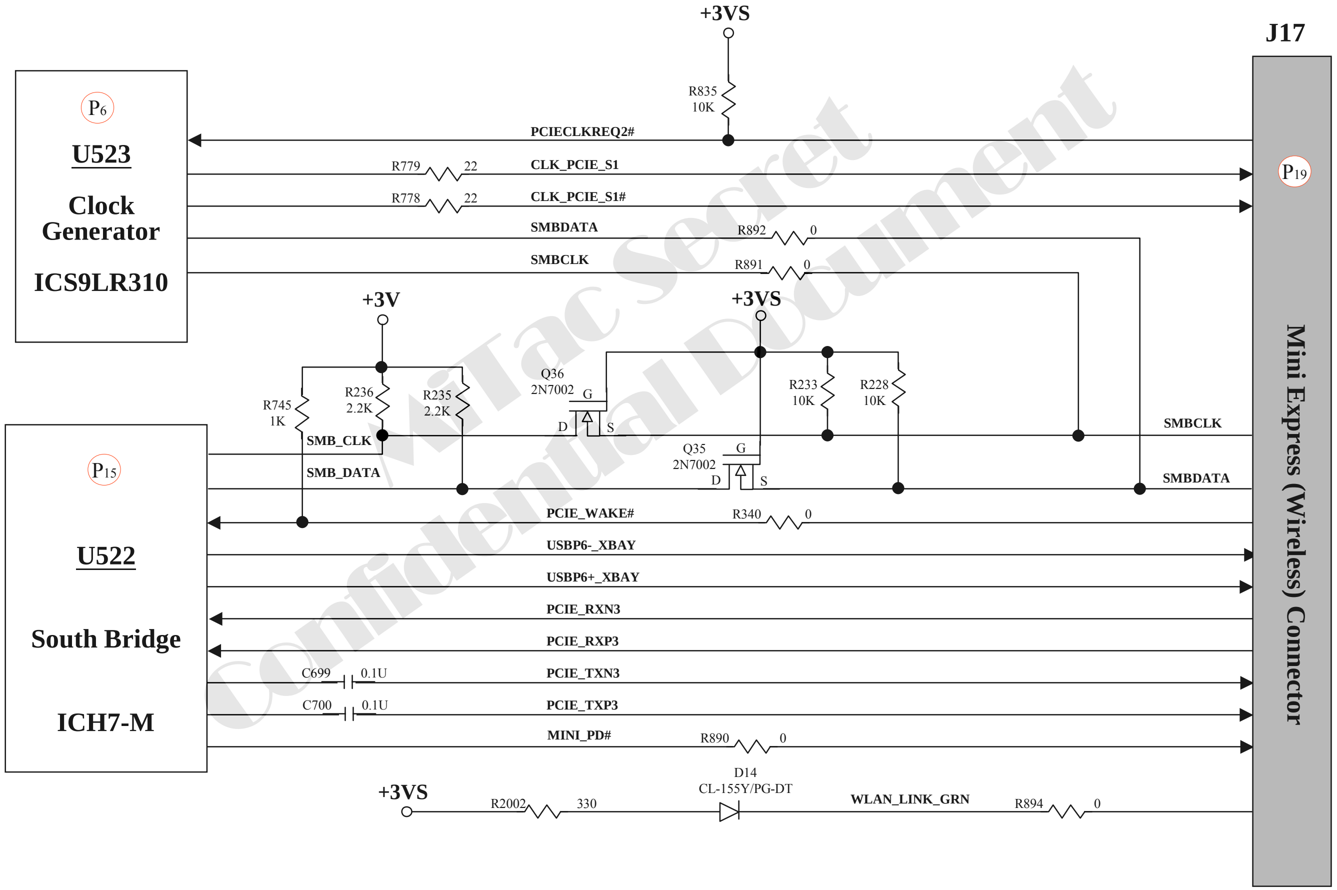
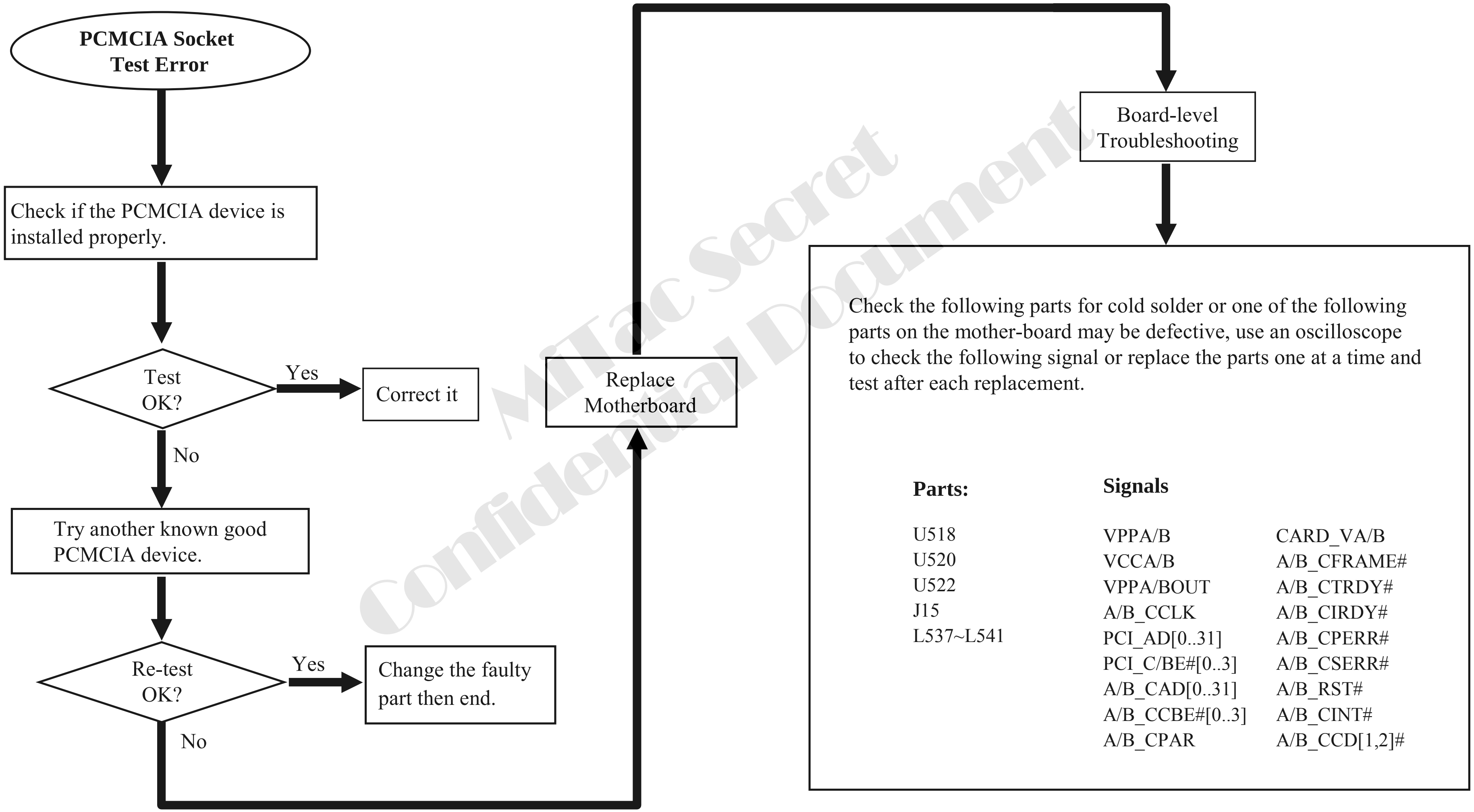
8.13 Mini Express (Wireless) Socket Test Error-2

An error occurs when a wireless card device is installed.


+3VS
J17
R835
10K
P6
U523
Clock
Generator
ICS9LR310
PCIECLKREQ2#
R779
22
CLK_PCIE_S1
R778
22
CLK_PCIE_S1#
P19
SMBDATA
R892
0
SMBCLK
R891
0
+3V
+3VS
Q36
2N7002
G
D
S
R745
1K
R236
2.2K
R235
2.2K
R233
10K
R228
10K
SMB_CLK
SMB_DATA
Q35
2N7002
G
D
S
SMBCLK
SMBDATA
Mini Express (Wireless) Connector
P15
U522
South Bridge
ICH7-M
PCIE_WAKE#
R340
0
USBP6-_XBAY
USBP6+_XBAY
PCIE_RXN3
PCIE_RXP3
C699
0.1U
PCIE_TXN3
C700
0.1U
PCIE_TXP3
MINI_PD#
R890
0
+3VS
R2002
330
D14
CL-155Y/PG-DT
WLAN_LINK_GRN
R894
0

8.14 PCMCIA Socket Test Error-1

An error occurs when a express card device is installed.


PCMCIA Socket Test Error
Check if the PCMCIA device is installed properly.
Test OK?
Yes
Correct it
No
Try another known good PCMCIA device.
Re-test OK?
Yes
Change the faulty part then end.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U518	VPPA/B	CARD_VA/B
U520	VCCA/B	A/B_CFRAME#
U522	VPPA/BOUT	A/B_CTRDY#
J15	A/B_CCLK	A/B_CIRDY#
L537~L541	PCI_AD[0..31]	A/B_CPERR#
	PCI_C/BE#[0..3]	A/B_CSERR#
	A/B_CAD[0..31]	A/B_RST#
	A/B_CCBE#[0..3]	A/B_CINT#
	A/B_CPAR	A/B_CCD[1,2]#

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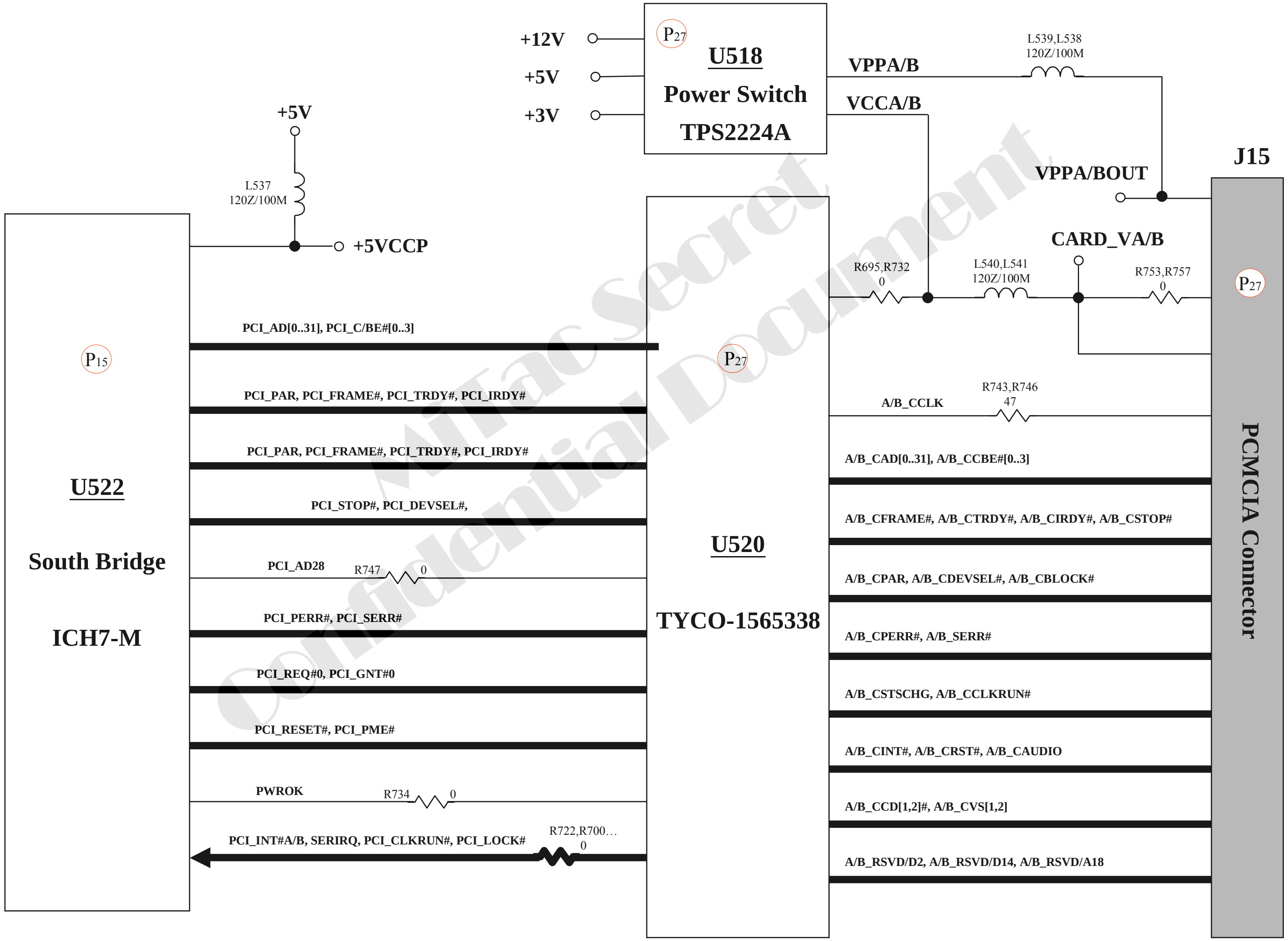
M230 N/B Maintenance

8.14 PCMCIA Socket Test Error-2

An error occurs when a express card device is installed.



+12V
+5V
+3V
P27
U518
Power Switch
TPS2224A
VPPA/B
VCCA/B
L539,L538
120Z/100M
J15
VPPA/BOUT
+5V
L537
120Z/100M
+5VCCP
CARD_VA/B
R695,R732
0
L540,L541
120Z/100M
R753,R757
0
P27
PCI_AD[0..31], PCI_C/BE#[0..3]
P15
P27
PCI_PAR, PCI_FRAME#, PCI_TRDY#, PCI_IRDY#
A/B_CCLK
R743,R746
47
PCI_PAR, PCI_FRAME#, PCI_TRDY#, PCI_IRDY#
A/B_CAD[0..31], A/B_CCBE#[0..3]
U522
PCI_STOP#, PCI_DEVSEL#,
A/B_CFRAME#, A/B_CTRDY#, A/B_CIRDY#, A/B_CSTOP#
U520
South Bridge
PCI_AD28
R747
0
A/B_CPAR, A/B_CDEVSEL#, A/B_CBLOCK#
PCMCIA Connector
PCI_PERR#, PCI_SERR#
TYCO-1565338
ICH7-M
A/B_CPERR#, A/B_SERR#
PCI_REQ#0, PCI_GNT#0
A/B_CSTSCHG, A/B_CCLKRUN#
PCI_RESET#, PCI_PME#
A/B_CINT#, A/B_CRST#, A/B_CAUDIO
PWROK
R734
0
A/B_CCD[1,2]#, A/B_CVS[1,2]
R722,R700…
0
PCI_INT#A/B, SERIRQ, PCI_CLKRUN#, PCI_LOCK#
A/B_RSVD/D2, A/B_RSVD/D14, A/B_RSVD/A18

9. Spare Parts List --1

Part Number	Description	Location(s)
791901160015	NB0;M230-4,53G,USB,S,16-D1-12	
796115030056	TF041-COVER;HOOK,BLACK,M220	
796115010024	TF041-SPRING;HOOK,M220	
796115000007	TF041-CORNER RUBBER;T-L,ASSY,	
796115000008	TF041-CORNER RUBBER;T-R,ASSY,	
796115000009	TF041-CORNER RUBBER;D-L,ASSY,	
796115000010	TF041-CORNER RUBBER;D-R,ASSY,	
796115010007	TF041-HOOK;LCD,SUS,M220	
796115030022	TF041-PARTITION;LCD CABLE,M22	
796115050010	TF041-BOX;HOUSING,BLUETOOTH,M	
796115050025	TF041-BOX;COVER,BLUETOOTH,M22	
796115060023	TF041-HOOK;LCD,RUBBER,M220	
796115090003	TF041-HOUSING;LCD,14.1,M220	
796115090004	TF041-BEZEL;LCD,14.1,M220	
796115020020	TF041-HINGE;ROT SHAFT,M220	
796115050032	TF041-HOOK,LCD,PLASTIC,M220	
796115050087	TF041-FIXTURE;INVER PCB CABLE	
342115000001	TF041-MAGNET;11.9*5.9*1.2MM.1	
796115074004	TF041-THERMAL PAD;INVERTER,M2	
796115050052	TF041-MYLAR;INVERTER,15",M220	
796115060109	TF041-WLAN/GPRS SPONGE;14"/15	
796115070055	TF041-3M;SCOTCH-GRIP,PLASTIC	
796115070079	TF041-DOUBLE TAPE;3M#9888T,4m	
796119070014	TF041-DUO-PAK,DP-420,OFF-WHIT	
796115070071	TF041-TAPE;3M,#1350,W1.5CM,66	

Part Number	Description	Location(s)
225600000422	TF041-POLYIMIDE TAPE;WIDE 20m	
346121200009	TF041-GASKET;ψ1.6,CA27,(FT)	
796121270051	TF041-DOW CORNING 3140 RTV SI	
796121270052	TF041-ADHESIVE SILICON RTV-31	
412116000002	TF041-INVERTER ASSY; 15.1" DA	
221800920001	TF041-CARTON;380MM*320MM*150M	
226114200001	TF041-PLASTIC EPE;ANTI-STATIC	
226800900001	TF041-SPONGE;370MM*310MM*10MM	
332110020190	TF041-WIRE;#20,UL1007,31MM,BL	
343111500001	TF041-Cu FOIL;T=0.05mm,23mmx5	
346111500001	TF041-INSULATOR;TAPE,CAPTON,T	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
411115000127	TF041-PWA;PWA-DA-1A09-I03 INV	
271071102313	TF041-TH-RES;1K ,1/16W,5% ,	R11
271071104310	TF041-TH-RES;100K ,1/16W,5% ,	R7
271071137012	TF041-TH-RES;137 ,1/16W,1% ,	R14A
271071163105	TF041-TH-RES;160K ,1/16W,1% ,	R13
271071202304	TF041-TH-RES;2K ,1/16W,5% ,	R12,R16
271071304103	TF041-TH-RES;301K ,1/16W,1% ,	R3
271071470103	TF041-TH-RES;4.32K,1/16W,1% ,	R10
271071511313	TF041-TH-RES;510 ,1/16W,5% ,	R15
271071563102	TF041-TH-RES;56K ,1/16W,1% ,	R6
271071753302	TF041-TH-RES;75K ,1/16W,5% ,	R8
271072433101	TF041-TH-RES;43.2K,1/10W,1% ,	R1
271072474102	TF041-TH-RES;470K ,1/10W,1% ,	R4,R5

9. Spare Parts List --2

Part Number	Description	Location(s)
271072822103	TF041-TH-RES;8.2K ,1/10W,1% ,	R14B
272003105402	TF041-TH-CAP;1U ,CR,25V ,10	C22,C7
272010680402	TF041-TH-CAP;68P ,CR,2KV,10%	C18
272013475403	TF041-TH-CAP;4.7U ,25V ,10%,1	C14A
272023475402	TF041-TH-CAP;4.7U ,25V ,10%,1	C1
272071105411	TF041-TH-CAP;1U ,10V ,10%,060	C10,C4
272071334404	TF041-TH-CAP;0.33U ,10V ,10%,	C2
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10	C12,C16,C6
272073223408	TF041-TH-CAP;0.022U,CR,25V ,1	C9
272075101408	TF041-TH-CAP;100P ,50V ,10%,0	C15B,C20,C21
272075103415	TF041-TH-CAP;0.01U ,50V,10%,	C11,C13,C3,C8
272075471415	TF041-TH-CAP;470P ,50V,10%,06	C17
272075472703	TF041-TH-CAP;4700P,50V ,+ -20	C15A,C5
272990100302	TF041-TH-CAP;10P,3000V,+- 5%,	C19
273001050263	TF041-XFMR;LH10,20/1720,270mH	T1
281101010004	TF041-TH-IC;MP1010BEF(LF),CCF	U1
291000020229	TF041-TH-CON;HDR,MA,2P*1,3.5M	J2
291000911101	TF041-TL-CON;HDR,MA,11P*1,1.2	CN1
295000010248	TF041-TH-FUSE;FAST,1.5A,63VDC	F1
316115000040	TF041-PCB;PWA-DA-1A09-I03 INV	R0A
242804400010	TF041-TH-LABEL;BAR CODE,20*5,	
361200003204	TF041-SOLDER PASTE;PF606-P;FO	
422116000002	TF041-CABLE ASSY;T/S BD TO IN	
411115100022	TF041-TH-PWA;PWA-M220.LCD&BLU	
271002000312	TF041-TH-RES;0 ,1/10W,5% ,	R107

Part Number	Description	Location(s)
271071103108	TF041-TH-RES;10K ,1/16W,1% ,	R109,R110
272011226706	TF041-TH-CAP;22U ,CR,10V,1206	C114
272075104710	TF041-TH-CAP;0.1U ,50V,+80-2	C115
284510321002	TF041-TH-IC;ADM1032ARZ-1,TEMP	U104
291000021410	TF041-TH-CON;HDR,MA,14P*1,1.2	J100
291000033003	TF041-TH-CON;RECT,COAXIAL,30P	J101
331040010023	TF041-TH-CON;HDR,5P*2,FM,1.27	J103
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
242600000676	TF041-LABEL;25*6MM,COMMON	
316116000005	TF041-TH-PCB;PWA-M230,TOUCH S	R00
242804400010	TF041-TH-LABEL;BAR CODE,20*5,	
361200003204	TF041-SOLDER PASTE;PF606-P;FO	
226116010001	TF041-SPONGE EPE;ANTI-STATIC,	
221801220102	TF041-CARTON;M/B,SHERWOOD-B,P	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
242600000566	TF041-LABEL;BLANK,7MM*7MM,PRC	
226683810101	TF041-CARTOON;L490,W320,FOR I	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	
796115060052	TF041-LCD RUBBER;35*10*9T,M22	
796115060053	TF041-LCD RUBBER;30*10*9T,M22	
796115070027	TF041-SPRING;LCD CU FOIL COND	
796115070069	TF041-DOUBLE TAPE;3M,#4609,4M	
413000020737	TF041-LCD;LTD141ECGA,14.1",EH	
413000020734	TF041-LCD;LTD141ECGA,14.1",XG	
796116070001	TF041-TEMPERED GLASS;14.1,POL	

9. Spare Parts List --3

Part Number	Description	Location(s)
796115160026	TF041-PORON;L32,100*20*2T,14"	
796115160027	TF041-PORON;SR-S 32P,60*15*2T	
796115160028	TF041-PORON;H32,50*6*3T,14" L	
796115160029	TF041-PORON;H32,100*6*3T,14"	
796115160034	TF041-PORON;H32,35*6*3T,14" L	
796115160036	TF041-PORON;L32 AND SR-S 32P,	
796115160037	TF041-PORON;SR-S 32P,297*4*2T	
796115160032	TF041-PORON;SR-S 32P,217*4*2T	
796115150021	TF041-MYLAR;LTD141ECGA,14",M2	
422116000015	TF041-CABLE ASSY;MB TO T/S &	
796115160011	TF041-GASKET; 733GT, A PART G	
796115070019	TF041-GASKET;I/O BD CONDUCT P	
796119002016	TF041-CONDUCTIVE TAPE;LCD CON	
332810018001	TF041-PWR CORD;125V,10A,3P,PV	
791921160005	TF041-AC ADAPTER ASSY; 90-264	
565111600001	TF041-S/W;CD ROM,SYSTEM DRIVE	
799001160001	TF041-Manual;USER'S,EN,M230	
796115070067	TF041-LOGO;BIG,M220	
796115070068	TF041-LOGO;SMALL,M220	
796115010025	TF041-NEEDLE;RESERT KEY,M220	
225600000421	TF041-TAPE;INSULATION,AC04,50	
230000030047	TF041-RIBBON;13CM*300M,LABEL	
242600000650	TF041-LABEL;25*10MM,POLYESTER	
242600000651	TF041-LABEL;25*10MM,3020F	
242600000652	TF041-LABEL;3.5"DISKETTE,BLAN	

Part Number	Description	Location(s)
242600000653	TF041-LABEL;MODEL,5M,MITAC	
230000030048	TF041-RIBBON;11CM*300M,PT800	
796119070006	TF041-TAPE;25MM*45M, CM34	
799001212004	TF041-MANUAL;BATTERY CAUTION,	
796119072005	TF041-LABEL;INTEL CORE DUO	
242670800148	TF041-LABEL;WINXP,ARTEMIS	
799001160003	TF041-Manual;Quick Start Guid	
796115030030	TF041-TOP CASE;HDD,M220	
796115050007	TF041-MYLAR;RIBBON HDD MODULE	
796115050056	TF041-MYLAR;HDD FRONT,M220	
412116000001	TF041-TH-PCB ASSY; SATA HDD A	
796116030002	TF041-BOTTOM-CASE;HDD,M230	
523450283097	TF041-TH-HDD DRIVE;120GB,MK-1	
796116060007	TF041-SPONGE;PORON SR-S 32P a	
796116060008	TF041-SPONGE;PORON H32,70*10*	
796116060009	TF041-SPONGE;PORON H32,90*10*	
796116060010	TF041-SPONGE;PORON SR-S 24P a	
796116060011	TF041-SPONGE;PORON H32,30*10*	
796116060012	TF041-SPONGE;PORON SR-S 24P,5	
796114960029	TF041-RUBBER KEY;KEYBOARD,ML9	
796115030029	TF041-BKT;TOP BKT,RUBBER-KB,M	
796115030003	TF041-BKT;RUBBER KBD,M220	
796115050051	TF041-MYLAR;RUBBER-KB,M220	
796115050055	TF041-MYLAR;PLATE,RUBBER-KB,M	
411116000065	TF041-TH-PWA;PWA-M230,KBD,LED	

9. Spare Parts List --4

Part Number	Description	Location(s)
411116000031	TF041-TH-PWA;PWA-M230,KBD LED	
332210000033	TF041-TL-CABLE;FLAT,P=1.0MM,P	
271001100301	TF041-TH-RES;100 ,1/10W,5% ,	R1,R2
294011200534	TF041-TH-LED;RED,H0.8,0603,C1	
316116000010	TF041-TH-PCB;PWA-M230,KBD LED	R01
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
796115000071	TF041-DOOR;PCMCIA,200MP,ASSY,	
796115000072	TF041-DOOR;BATT,200MP,ASSY,M2	
796115000073	TF041-DOOR;CD ROM,200MP,ASSY,	
796115000074	TF041-DOOR;HDD,200MP,ASSY,M22	
796115000006	TF041-ASSY;SIM-CARD MOUDLE,M2	
796115010004	TF041-RINGS;BELT,M220	
796115020001	TF041-BKT;BATT-PCMCIA DOOR,M2	
796115020002	TF041-BKT;CD ROM-HDD DOOR,M22	
796115020003	TF041-BKT;SPEAKER,M220	
796115020004	TF041-BKT;TOUCH PAD,M220	
796115020005	TF041-BKT;DC-DOOR,M220	
796115020009	TF041-BKT;CRT-DOOR,M220	
796115020010	TF041-BKT;PRINT-PORT-DOOR,M22	
796115020011	TF041-BKT;USB-PS2-DOOR,M220	
796115030002	TF041-BKT;POWER BUTTON,M220	
796115030026	TF041-COVER;HINGE,M220	
796115050001	TF041-COVER;PALM-REST,M220	
796115050004	TF041-LED;FN-DISPLAY,M220	
796115050005	TF041-LED;POWER,M220	

Part Number	Description	Location(s)
796115050022	TF041-LENS;IR,M220	
796115050026	TF041-MYLAR;LED,HINGE-COVER,M	
796115050028	TF041-MYLAR;TP-PCB,M220	
796115050029	TF041-MYALR;RELEASE,HANDLE,DV	
796115060006	TF041-CORNER RUBBER;L-R,MAIN	
796115060007	TF041-CORNER RUBBER;L-F,MAIN	
796115060008	TF041-CORNER RUBBER;R-R,MAIN	
796115060009	TF041-CORNER RUBBER;R-F,MAIN	
796115060014	TF041-RUBBER;SPEAKER,M220	
796115060015	TF041-BUTTON;POWER,M220	
796115060030	TF041-RUBBER;STOPER,SIM,COVER	
796115060031	TF041-RUBBER;MOUSE,R-L,M220	
796115060032	TF041-RUBBER;SMT,SWITCH,DOCKI	
796115090002	TF041-COVER;DDR,M220	
411116000007	TF041-TH-PWA;PWA-M230, LED BD	
271071471308	TF041-TH-RES;470 ,1/16W,5% ,	HR1,HR2,HR3,HR5,HR6,HR7
291000151005	TF041-TH-CON;FPC/FFC,10P,1MM,	HJ1
294011200523	TF041-TH-LED;GRN,H1.5,1206,PG	HD2,HD3,HD4,HD5
316116000004	TF041-TH-PCB;PWA-M230,LED BD	R00
294011200504	TF041-TH-LED;YEL/GRN,H1.1,L3.	HD1
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
226800020001	TF041-BOX;PET,1/20,SEC-V6,GPP	
221800020002	TF041-CARTON;425*310H240,SEC-	
226683810101	TF041-CARTOON;L490,W320,FOR I	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	

9. Spare Parts List --5

Part Number	Description	Location(s)
422116000007	TF041-CABLE ASSY;MBD TO LED B	
339111000089	TF041-SPEAKER ASSY;Φ23mm,2W,	
339111000090	TF041-SPEAKER ASSY;Φ23mm,2W,	
796115070002	TF041-THERMAL PAD;DDR,M220	
344600001135	TF041-IC CARD CON PART;68P*2,	
411116000056	TF041-TH-PWA;PWA-M230 NAPA,IO	
272075339907	TF041-TH-CAP;3.3P ,CR,50V ,+-	C1,C12,C13,C15,C49,C5
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	C2,C42
272102104708	TF041-TH-CAP;0.1U ,16V,+80-2	
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,06	C520,C538
272105102421	TF041-TH-CAP;1000P,CR,50V,10%	C500
272030102414	TF041-TH-CAP;1000P,3KV,10%,18	C508,C509,C550
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D3
288100112005	TF041-TH-DIODE;EC11FS2-TE12L,	D4
288105435001	TF041-TH-STEERING DIODE;SRV05	
288104148020	TF041-TH-DIODE;RLS4148,200MA,	D16
288100402002	TF041-TL-DIODE ; ESD. V-PORT-	
273000500183	TF041-TH-FERRITE CHIP;120OHM/	
295000010259	TF041-TH-FUSE;1.1A/6V,POLY SW	F1,F501
297010400001	TF041-TH-SW; PUSH BUTTON, SPS	HSW1
291000005017	TF041-TH-CON;RECT,COAXIAL,50P	J1
291000003015	TF041-TH-CON; 30P,6902-E30N-0	J2
331040005015	TF041-TH-CON;STEREO JACK,5P,R	J503
291000810223	TF041-TH-CON;PHONE JACK,2P,H1	J504
291000020820	TF041-TH-CON;RJ45,WO/LED,8P,H	J505

Part Number	Description	Location(s)
331840010019	TF041-TH-CON;STEREO JACK,10P,	J506
291000011228	TF041-TH-CON;HDR,MA,60P*2,0.8	J507
291000020233	TF041-TL-CON;HDR,MA,2P*1,1.25	J508
273000500182	TF041-TH-CHOKE COIL;120OHM/10	
297011000001	TF041-TH-SW;TACT,SPST,BY MAGN	Q1
288200144034	TF041-TH-TRANS;DDTA144WKA,PNP	Q3
288200144029	TF041-TH-TRANS;DTC144WK,NPN,S	Q4
271061103114	TF041-TH-RES;10K ,1/16W,1% ,	R1,R5,R514,R515,R545
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,	R2
271061473502	TF041-TH-RES;47K ,1/16W,5% ,	R10
271061104108	TF041-TH-RES;100K ,1/16W,1% ,	R547
271002000312	TF041-TH-RES;0 ,1/10W,5% ,	R25,R544,R546
271061750105	TF041-TH-RES;75,1/16W,1%,0402	
284501284006	TF041-TH-IC;PACSZ1284-02QR,QS	U1
288100006006	TF041-TH-DIODE ARRAY;PACDN006	U3
286303311001	TF041-TH-IC;ADM3311EARU TSSOP	U501
273000610054	TF041-TH-FERRITE ARRAY;120OHM	FA1
316116000016	TF041-TH-PCB;PWA-M230 NAPA,IO	R01
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
288200144030	TF041-TH-TRANS;DDTC144TKA,N-M	Q2
291000012808	TF041-TH-CON;HDR,14P*2, 0.8MM	J510
288115112001	TF041-TH-DIODE ; ESD. V-PORT-	D500,D501
286301117110	TF041-TH-IC;APL1117-VC-TRL,1A	U503
273001050206	TF041-TL-XSFORMER;100/1000 BA	U500
273000500187	TF041-TH-FERRITE CHIP;120OHM/	

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Part Number	Description	Location(s)
272073104712	TF041-TH-CAP;0.1U,25V,10%,060	
272101016401	TF041-TH-CAP;.1U ,CR,10V,10%	C504,C506,C522,C523
271071101107	TF041-TH-RES;100 ,1/16W,1% ,	R549,R550
271061100103	TF041-TH-RES;10,1/16W,1%,0402	R548
270140000008	TF041-TH-THYRISTOR;280V,5.6X3	S500
288106830001	TF041-TH-TVS DIODE ; RSB6.8S-	
361200003204	TF041-SOLDER PASTE;PF606-P;FO	
225118020001	TF041-TAPE;SOLDER PREVENT,1/2	
288100603005	TF041-TL,DIODE ; ESD. MLVS-06	D19,D573
288103050001	TF041-TH-ESD DIODE; PD03S050	
273030300119	TF041-TH;FERRITE BEAD 90OHM/1	L10,L4,L512,L8
272105390401	TF041-TH-CAP;39P,50V,+-10%,04	C530,C532,C534,C536
272071105412	TF041-TH-CAP;1U,10V,10%,0603,	C552
272075471422	TF041-TH-CAP;470P,CR,50V,10%,	C47,C48
288103180001	TF041-TH-ESD DIODE; PD03S180H	D17,D18,D2
288202301008	TF041-TH-TRANS;SI2301BDS,P-MO	Q500
796116070007	TF041-SPRING;TCSBB40-5,USB GN	SP2,SP3
796116070005	TF041-SPRING;TCSBD30-5,AUDIO	SP1
796116050003	TF041-MYLAR;13mm*26mm*0.4mm	
331040025003	TF041-TH-CON; D,FM,25P,2.77,R	J500
331040015004	TF041-TH-CON;D,FM,15P,2.29,R/	J501
331040009005	TF041-TH-CON;D,MA,9P,2.775,R/	J502
221680820005	TF041-CARTON;BATTERY,CAIMAN,P	
221680850002	TF041-PARTITION;BATTERY,MARLI	
221680850003	TF041-PARTITION;TOP/BTM,BATTE	
222687630001	TF041-PE BUBBLE BAG;BATTERY,G	
226687620001	TF041-SPONGE;320*290*10,CAIMA	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	
242600000566	TF041-LABEL;BLANK,7MM*7MM,PRC	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
422116000009	TF041-FFC ASSY;TOUCH PAD,M230	
422116000013	TF041-CABLE ASSY;NAPA MBD TO	
797726443194	TF041-STANDOFF;#4-40L5.5D5,H/	
796115000075	TF041-ASSY;CD ROM,RELEASE MOD	
796116000005	TF041-TOP HOUSING ASSY;MAIN-S	
796116090001	TF041-TOP HOUSING; MAIN-SYS,M	
796115020018	TF041-BKT;HOOK,FIX,M220	
796115090005	TF041-COVER;X-BAY,M220	
796115020019	TF041-SPRING;RELEASE,HANDLE,M	
411116000010	TF041-TH-PWA;PWA-M230, TRACK	
271071103310	TF041-TH-RES;10K ,1/16W,5% ,	R500,R501
272005105402	TF041-TH-CAP;0.1U,CR,50V,10%,	C501
272011106714	TF041-TH-CAP;10U ,10V,+80-20	C500
291000151219	TF041-TH-CON;FPC/FFC,12P,0.5M	J500,J501
297040105039	TF041-TH-SW;PUSH BUTTON,SPST,	SW1,SW2,SW3,SW4
316116000006	TF041-TH-PCB;PWA-M230,TRACK P	R00
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
226800020001	TF041-BOX;PET,1/20,SEC-V6,GPP	
221800020002	TF041-CARTON;425*310H240,SEC-	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	

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Part Number	Description	Location(s)
796115030019	TF041-RELEASE;HANDLE,DVD,M220	
796115000028	TF041-COVER ASSY;LCD-KEY-CONN	
796115050031	TF041-HOLDER PROTECT HOOK,M2	
796115060046	TF041-RUBBER;DDR,BOTTOM,M220	
796115060049	TF041-RUBBER;LCD KEYBOARD,CAB	
796115050035	TF041-PLATE_TP_ALPS_M220	
796115050034	TF041-MYLAR;BATT SIDE-WALL,M2	
796115070024	TF041-GASKET;I/O BRACKET,W22.	
796115070026	TF041-GASKET;C-PART CD ROM TO	
796115070019	TF041-GASKET;I/O BD CONDUCT P	
796115050038	TF041-MYLAR;7-LED,DISPLAY,M22	
796150063002	TF041-GRIP GROUP;W150	
796115070031	TF041-GASKET; CAP. TOUCH PAD,	
796115050033	TF041-MYLAR;BATT,M220	
796115020017	TF041-BKT;COVER;SIM-CARD,M220	
796115010018	TF041-SCR;HANDLE,M3L13.5,M220	
796115050049	TF041-MYLAR;HDD_SIDE,M220	
796115050048	TF041-MYLAR;HDD_UPPER,M220	
796115060088	TF041-RUBBER;ANTENNA,X-BAY,M2	
796115070058	TF041-CLOTH;SPEAKER,M220	
796115060013	TF041-RUBBER;RELEASE HANDLE,M	
796115070060	TF041-GASKET;HDD GAP,W10,H1.0	
796116000004	TF041-BOTTOM COVER ASSY;MAIN-	
796116000002	TF041-BOTTOM COVER;PAINT,M230	
796115070070	TF041-AL FOIL; TOUCH PAD BRAC	

Part Number	Description	Location(s)
796115070066	TF041-LABEL;COVER DDR,M220	
796115100009	TF041-RUBBER FOOT;MAIN-SYS,M2	
796115100010	TF041-CAP ASSY;COM PORT,M220	
796115100011	TF041-CAP ASSY;DC-IN,M220	
796115100012	TF041-CAP ASSY;PHONE-JACK,M22	
796115100013	TF041-CAP ASSY;PRINT-PORT,M22	
796115100014	TF041-CAP ASSY;RJ11-RJ45,M220	
796115100016	TF041-CAP ASSY;CRT,M220	
796116060003	TF041-RUBBER;DDR,M230	
442802200003	TF041-TOUCHPAD MODULE;TM61PUF	
796115160017	TF041-NANNEX;COVER,TL4401 16*	
796115160018	TF041-NANNEX;COVER,TL4403 16*	
346121200009	TF041-GASKET;ψ1.6,CA27,(FT)	
411116000052	TF041-TH-PWA;PWA-M230,NAPA M/	
331000005046	TF041-TH-CON;RP MMCX CONNECTO	J4,J5,J6,J7
331040004039	TF041-TH-CON;HDR,SHROUD,MA,4P	J10,J11
796115000001	TF041-HOUSING;POGO,MODULE,ASS	J503
331000004089	TF041-CON;BATTERY,0402A120,4P	PJ1
331000007082	TF041-CON;BATTERY,7P,MA,2.5MM	PJ2
331000005033	TF041-TH-CON;BATTERY,5P,MA,5.	PJ3
481116000001	TF041-F/W ASSY;SYS/VGA BIOS,M	U512
421118200001	TF041-WIRE ASSY;BIOS,BATTERY	J16
411116000054	TF041-TH-PWA;PWA-M230,NAPA M/	
272101015402	TF041-TH-CAP;1U,6.3V,+-10%,04	
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	

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9. Spare Parts List --8

Part Number	Description	Location(s)
272101104415	TF041-TH-CAP;0.1U ,CR,10V,10	
272102104708	TF041-TH-CAP;0.1U ,16V,+80-2	
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,06	
272431157518	TF041-TH-CAP;150U ,TPC,6.3V,2	
272011226706	TF041-TH-CAP;22U ,CR,10V,1206	
272001106404	TF041-TH-CAP;10U,6.3V ,10%,08	
272105101313	TF041-TH-CAP;100P ,50V ,5%,04	C61,C612,C65,PC29,PC30
272401107507	TF041-TL-CAP;100U,POSCAP,4V,2	
272431477003	TF041-TH-CAP;470U,2.5V,2R5TPE	
272105470403	TF041-TH-CAP;47P ,50V ,+ -10	
272102224401	TF041-TH-CAP;.022U,16V,+-10%,	
272103103407	TF041-TH-CAP;0.01U ,CR,25V ,1	
272101474703	TF041-TH-CAP; 0.47U ,CR,10V,+	
272431227006	TF041-TH-CAP;220uF,4V,7343,25	C372,C743,C781,C790
272105392502	TF041-TH-CAP;3900P,50V,+/-20%	C377,C378,C808,C812
272105102421	TF041-TH-CAP;1000P,CR,50V,10%	
272001106517	TF041-TH-CAP;10U,10V,+80-20%,	C507,C508
272073104712	TF041-TH-CAP;0.1U,25V,10%,060	
272105270305	TF041-TH-CAP;27P ,50V ,5%,04	C537,C540
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,1	
272072474403	TF041-TH-CAP;0.47U,16V,10%,06	
272072473409	TF041-TH-CAP;0.047U,16V ,10%,	C576
272105222411	TF041-TH-CAP;2200P,50V ,+/-10	C649
272105220404	TF041-TH-CAP;22P ,50V ,+ -10	
272101224702	TF041-TH-CAP;0.22U ,10V ,+80-	C237,C265,C722,C73

Part Number	Description	Location(s)
272102473404	TF041-TH-CAP;0.047U,16V,10%,0	
272105390401	TF041-TH-CAP;39P,50V,+-10%,04	C764,C765
272105180308	TF041-TH-CAP;18P ,50V ,+/-5%	C817,C818
288100603003	TF041-TH-DIODE;ESD,V-PORT-060	D11,D15,D506,D515
288100561004	TF041-TH-DIODE;ESD MMBZ5V6ALT	D20
288100054035	TF041-TH-DIODE;BAT54C,SCHOTTK	
294011200536	TF041-TH-LED;YEL/GRN,H1.1,L3.	D14,D32,D36,D37
294011200502	TF041-TH-LED;YEL,H1.5,1206,11	D33,D34
288105556002	TF041-TH-DIODE;BZV55-C5V6,ZEN	D501
288104148020	TF041-TH-DIODE;RLS4148,200MA,	D507,D518
288100099015	TF041-TH-DIODE;BAV99,70V,450M	D509,D514,D516
288100541004	TF041-TH-DIODE;BAT54ALT1,COM.	
295000010218	TF041-TH-FUSE;FAST,2A,63VDC,1	F1
295000010206	TF041-TH-FUSE;NORMAL,6.5A/32V	F2,PF501
291000010630	TF041-TH-CON;HDR,FM,3P*2,2.0M	J1
291000000905	TF041-TH-CON;MINI IEEE1394B,R	J2
291000011229	TF041-TH-CON;HDR,FM,60P*2,0.8	J3
291000141004	TF041-TH-CON;FPC/FFC,10P,1MM,	J8
291000012806	TF041-TH-CON;HDR,14P*2, 0.8MM	J9
291000025038	TF041-TH-CON;HDR,25P*2,FM,.8M	J12
291000018402	TF041-TH-CON;HDR,42P*2,0.8MM,	J13
291000011227	TF041-TL-CON;WFR,MA,12P,1.25M	J510
291000251504	TF041-TH-CON;IC CARD,75P*2,FM	J15
291000020233	TF041-TL-CON;HDR,MA,2P*1,1.25	J16,J507,J508
291000255201	TF041-TH-CON;MINI PCI-EXPRESS	J17

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Part Number	Description	Location(s)
291000025204	TF041-TL-CON;D,MA,52P,.635MM,	J18
291000921202	TF041-TH-CON;MDC 12P,H=5MM,PI	J19
297150100015	TF041-TH-SW;SWITCH,RF SLIDE S	J501,J502
291000612036	TF041-TH-CON;DDR2 STD SOCKET	J504
291000612034	TF041-TH-DIMM SOCKET;DDRII RE	J505
291000150815	TF041-TL-CON;FPC/FFC,8P,1MM,R	J506
291000151219	TF041-TH-CON;FPC/FFC,12P,0.5M	J509
273000500189	TF041-TH-CHOKE COIL;90OHM/100	L18,L22
273000990296	TF041-TH-INDUCTOR;10UH,+-20%,	L27,L28
273000500184	TF041-TH-FERRITE CHIP;600OHM/	L503,L505
272075102419	TF041-TH-CAP;1000P,CR,50V,10%	
272075102424	TF041-TH-CAP ;0.1U CR 50V 10%	
272075101408	TF041-TH-CAP;100P ,50V ,10%,0	PC13,PC21
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,1	PC16,PC20,PC527,PC589
272043226507	TF041-TH-CAP;22U ,25V ,+-20%,	PC539,PC540
272075152405	TF041-TH-CAP;1500P,CR,50V,10%	PC518
272075100404	TF041-TH-CAP;10P ,50V ,10%,0	PC519
272431336001	TF041-TH-CAP;330uF,6.3V,7343,	
272003105402	TF041-TH-CAP;1U ,CR,25V ,10	
288100540006	TF041-TH-DIODE;MBR0540_NL,1A,	
288105232007	TF041-TH-DIODE;MMSZ5232B,5.6V	
288100034012	TF041-TH-DIODE;SSA34,40V,3A,S	
288105252004	TF041-TH-DIODE;MMSZ5252B,24V,	PD514
295000010243	TF041-TH-FUSE;NANO,10A/125V,R	PF502,PF503,PF504
273000990377	TF041-TH-INDUCTOR;0.82UH,FDU1	PL509,PL512

Part Number	Description	Location(s)
273000990374	TF041-TH-INDUCTOR;4.7UH,D104C	
273000990375	TF041-TH-INDUCTOR;4.7UH,FDV06	PL513,PL518,PL519
288227002024	TF041-TH-TRANS;2N7002LT1,N-CH	
288207832004	TF041-TH-TRANS;IRF7832PBF,N-M	
288207821006	TF041-TH-TRANS;IRF7821PBF,N-M	
288200144029	TF041-TH-TRANS;DTC144WK,NPN,S	
288206679005	TF041-TH-TRANS;FDS6679_NL,P-M	
288204835008	TF041-TH-TRANS;SI4835BDY-T1-E	PQ523,Q14,Q22
288204832002	TF041-TH-TRANS;SI4832DY,N-MOS	PQ528
288203415002	TF041-TH-TRANS;AO3415,P-MOSFE	PU501
271061104108	TF041-TH-RES;100K ,1/16W,1% ,	
271061100103	TF041-TH-RES;10,1/16W,1%,0402	
271079474101	TF041-TH-RES;470K,1/10W,1% ,0	
271061203112	TF041-TH-RES;20K ,1/16W,1% ,	
271071403101	TF041-TH-RES;40.2K ,1/16W,1%	PR5
271061000003	TF041-TH-RES;0 ,1/16W,0402	
271071752105	TF041-TH-RES;7.5K,1/16W,1%,06	PR20,PR38,PR8,PR9
271061103114	TF041-TH-RES;10K ,1/16W,1% ,	
271061105104	TF041-TH-RES;1M,1/16W,1% ,040	
271061101109	TF041-TH-RES;100 ,1/16W,1% ,	
271072223101	TF041-TH-RES;22K ,1/10W,1% ,0	PR22
271061102113	TF041-TH-RES;1K ,1/16W,1% ,	
271072300331	TF041-TH-RES;300K ,1/10W,5% ,	PR535,PR540,PR55
271046017302	TF041-TH-RES;.001,2W,5%,2512,	PR503,PR514
271013221302	TF041-TH-RES;220 ,1/4W,5% ,1	PR507,PR568

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Part Number	Description	Location(s)
271071133104	TF041-TH-RES;13.3K,1/16W,.1%,	PR509
271072118311	TF041-TH-RES;118K ,1/10W,1% ,	PR510
271071513102	TF041-TH-RES;51K ,1/16W,1% ,	PR512
271072113312	TF041-TH-RES;113K ,1/10W,1% ,	PR516
271071184103	TF041-TH-RES;180K ,1/16W,1% ,	PR527
271061474304	TF041-TH-RES;470K ,1/16W,5% ,	PR529,R25,R343
271045029102	TF041-TH-RES;.02 ,1W,1%,2512,	PR531
271071287114	TF041-TH-RES;287K ,1/16W,1% ,	PR532,PR571
271061220105	TF041-TH-RES;22 ,1/16W,1% ,	
271061333304	TF041-TH-RES;33K ,1/16W,5% ,0	
271046257104	TF041-TH-RES;.025 ,2W ,1% ,25	PR562
271072372101	TF041-TH-RES;37.4K ,1/10W,1%	PR563
271071121217	TF041-TH-RES;12.1K,1/16W,1% ,	PR564
271071153105	TF041-TH-RES;15K ,1/16W,1% ,	PR567
271071150104	TF041-TH-RES;15 ,1/16W,1% ,06	PR576
271071562309	TF041-TH-RES;5.6K ,1/16W,5% ,	PR520,PR525,PR582
271071152107	TF041-TH-RES;1.5K ,1/16W,1% ,	PR586
271071283105	TF041-TH-RES;28K ,1/16W,1% ,	PR588
271072822102	TF041-TH-RES;8.2K ,1/10W,1% ,	PR594
286301485001	TF041-TH-IC;SC1485,PWM,TSSOP-	PU1,PU503
286300452001	TF041-TH-IC;SC452,PWM CONTROL	PU2
288204800008	TF041-TH-TRANS;SI4800DY,N-MOS	PU3,PU504,Q2
282574405205	TF041-TH-IC;74HC4052MX_NL,DUA	PU4
286302731001	TF041-TH-IC;LM2731YMF,Boost C	PU502
286000864002	TF041-TH-IC;OZ864,DUAL BATT C	PU506

Part Number	Description	Location(s)
286300480001	TF041-TH-IC;SC480,PWM-DDR2,ML	PU507
286302951020	TF041-TH-IC;LP2951ACM NOPB,Vo	PU509
286300809025	TF041-TH IC;ADM809SART-REEL7	PU510
286300055003	TF041-TH-IC;TC55,3.3V,250mA,R	PU511
288200144030	TF041-TH-TRANS;DDTC144TKA,N-M	
288200069011	TF041-TH-TRANS;BCP69,PNP,SOT-	Q10,Q3
288200645001	TF041-TH-TRANS;FDC645N_NL,5.5	Q519,Q521
271611103305	TF041-TH-RP;10K*4 ,8P ,1/16W,	RP1,RP501
271621103306	TF041-TH-RP;10K*8 ,10P,1/32W,	RP502
271621472306	TF041-TH-RP;4.7K*8,10P,1/32W,	RP2
271071228306	TF041-TH-RES;2.2 ,1/16W,5% ,	R2,R772,R866
271061471308	TF041-TH-RES;470 ,1/16W,5% ,	R11,R179
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,	
271061560106	TF041-TH-RES;56.2,1/16W,1%,04	R35,R36,R37,R39
271061394307	TF041-TH-RES;390K ,1/16W,5% ,	R61
271061221318	TF041-TH-RES;220 ,1/16W, 5%,	R139,R2020,R67
271061632102	TF041-TH-RES;6.34K,1/16W,1% ,	R107
271061270104	TF041-TH-RES;27.4 ,1/16W, 1%	R129,R687
271061540102	TF041-TH-RES;54.9 ,1/16W,1% ,	
271061272105	TF041-TH-RES;2.7K ,1/16W,1% ,	R715,R716
271061822307	TF041-TH-RES;8.2K ,1/16W,5% ,	
271061202104	TF041-TH-RES;2K ,1/16W,1% ,	R186,R555
271061473103	TF041-TH-RES;47K ,1/16W,1% ,	
271061251102	TF041-TH-RES;255,1/16W,1%,040	R225
271061221107	TF041-TH-RES;221,1/16W,1%,040	R232,R769

9. Spare Parts List --11

Part Number	Description	Location(s)
271061201107	TF041-TH-RES;200 ,1/16W, 1%,	R239,R539
271061560306	TF041-TH-RES;56 ,1/16W,5% ,	
271061240102	TF041-TH-RES;24.9,1/16W,1% ,0	
271061334103	TF041-TH-RES;332K,1/16W,1%,04	R317
271061800101	TF041-TH-RES;80.6,1/16W,1%,04	R320,R324
271061390309	TF041-TH-RES;39, 1/16W, 5%,0	
271061204104	TF041-TH-RES;200K ,1/16W,1% ,	R554
271061331313	TF041-TH-RES;330,1/16W,5% ,04	R1004,R1010,R1011,R2001
271061492102	TF041-TH-RES;4.99K,1/16W,1% ,	R185,R677
271061750105	TF041-TH-RES;75,1/16W,1%,0402	
271061131109	TF041-TH-RES;130 ,1/16W,1% ,	R611
271071101107	TF041-TH-RES;100 ,1/16W,1% ,	R639,R640
271061152502	TF041-TH-RES;1.5K ,1/16W,5% ,	R646,R658
271071100103	TF041-TH-RES;10 ,1/16W,1% ,	R655,R727
271061510306	TF041-TH-RES;51, 1/16W, 5%,0	R683
271071000312	TF041-TH-RES;0 ,1/16W,5% ,	
271061010102	TF041-TH-RES;1,1/16W,1%,0402,	R723,R766
271061470502	TF041-TH-RES;47 ,1/16W,5% ,	R743,R746
271061330311	TF041-TH-RES;33 ,1/16W,5% ,	
271061222104	TF041-TH-RES;2.2K,1/16W,1%,04	
271061433306	TF041-TH-RES;43K ,1/16W,5% ,0	R793,R802
271061106308	TF041-TH-RES;10M ,1/16W,5% ,	R882
271071220308	TF041-TH-RES;22 ,1/16W,5% ,	R883
297120100019	TF041-TH-SW;SMT,SPST,8P,1.27P	SW1
297040200013	TF041-TH-SW;PUSH BUTTON,DPDT,	SW2

Part Number	Description	Location(s)
288003602002	TF041-TH-FIR; HSDL-3602-007 F	U1
284510268002	TF041-TH-IC;SIO10N268,SMSC SU	U4
284505752007	TF041-TH-IC;BCM5752;GIGA Bit	U5
284501394004	TF041-TH-IC;1394B PHY,TSB81BA	U6
286374131002	TF041-TH-IC;SN74LVC1G3157-DCK	U10,U11,U8
284501394003	TF041-TH-IC;1394B CONTROLLER	U9
282074338003	TF041-TH-IC;74CBTD3384,10 BIT	U12
481116000002	TF041-F/W ASSY;KBD CTRL,H8,M	U13
286369229003	TF041-TH-IC;G692L293Tf,RESET	U14
281307085005	TF041-TH-IC;NC7SZ08P5,2-INPUT	U15,U16,U2001,U503
286301022001	TF041-TH IC;ADM1022ARQ QSOP-1	U17
282000302001	TF041-TH-IC;LIS3L02DQ,G-SENSO	U18
286104890003	TF041-TH-IC;AUDIO AMPLIFIER,L	U501
284500260006	TF041-TH-IC;ALC260,AUDIO CODE	U502
286391674003	TF041-TH-IC;RT9167-47PB,LDO,S	U504
286100212002	TF041-TH-IC;TPA0212,AMPLIFIER	U507
282074212002	TF041-TH-IC;SN74LVC2G125,DUAL	U508
286302545003	TF041-TL-IC;MIC2545A-1YMTR,US	U511,U517
291000613223	TF041-TH-IC SOCKET;32P,PLCC,T	U512
286301117110	TF041-TH-IC;APL1117-VC-TRL,1A	U514
284510321002	TF041-TH-IC;ADM1032ARZ-1,TEMP	U516
286302224001	TF041-TH-IC;TPS2224A,CARDBUS	U518
284501520004	TF041-TH-IC;PCI1520,PCI/CARDB	U520
284509310001	TF041-TH-IC;ICS9LPR310, LOW P	U523
282574164008	TF041-TH-IC;74VHC164,SIPO REG	U526

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Part Number	Description	Location(s)
274012500430	TF041-TH-XTAL;25MHZ,30PPM,18P	X501
274040304401	TF041-TH-OSC;98.304MHZ,3.3V,7	X502
274011000412	TF041-TH-XTAL;10M,30PPM,16PF,	X503
274011431467	TF041-TH-XTAL;14.318MHZ,16PF,	X504
274013275401	TF041-TH-XTAL;32.768KHZ,20PPM	X505
316116000015	TF041-TH-PCB;PWA-M230,NAPA M/	R02
284500007017	TF041-TH-IC;ICH7M,SOUTH BRIDG	U522
284500945004	TF041-TH-IC;INTEL 945GM GMCH,	U521
273000130360	TF041-TH-FERRITE CHIP;120OHM/	
283411600001	TF041-TH-IC;FLASH,AT45DB021B,	U506
294011200503	TF041-TH-LED;RED/GRN,H1.1,L3.	D31
288202303008	TF041-TH-TNANS;SI2303,P-MOSFE	PQ1,Q39,Q520,Q524
272071105412	TF041-TH-CAP;1U,10V,10%,0603,	
273000150374	TF041-TH-FERRITE CHIP;120OHM/	
271061223106	TF041-TH-RES;22.1K,1/16W,1% ,	PR15
271071134102	TF041-TH-RES;130K ,1/16W,1% ,	PR24
271071303105	TF041-TH-RES;30.1K,1/16W,1%,0	PR37
272075680307	TF041-TH-CAP;68P ,50V ,5% ,0	PC22
271061432102	TF041-TH-RES;4.3K,1/16W,1%,04	R761
286300320002	TF041-TL-IC;PI3USB20 SWITCH 4	U515
284180786068	TF041-TH-IC;CPU,YONAH,LV,1.66	U513
281307125007	TF041-TH-IC;NC7SZ125,SINGLE,S	U3
271071333102	TF041-TH-RES;33K ,1/16W,1% ,	R631
271061196215	TF041-TH-RES;19.6K,1/16W,1%,0	R633
272075471422	TF041-TH-CAP;470P,CR,50V,10%,	PC534

Part Number	Description	Location(s)
271061490102	TF041-TH-RES;49.9 ,1/16W,1% ,	
272075102505	TF041-TH-CAP;1000P,50V ,+/-20	C80
288104024001	TF041-TH,DIODE,TVS ARRAY;40PF	D300,D504
288179301001	TF041-TH-IC;TPS79301DBVR ,TI,	U510
272105271406	TF041-TH-CAP;270P ,50V,+-10%,	C21,C94
271061681308	TF041-TH-RES;680 ,1/16W,5% ,	PR58
272433156506	TF041-TH-CAP;15U,25V,20%,60M,	
282574132012	TF041-TH-IC;74AHCT1G32,SINGLE	U2000
271061122107	TF041-TH-RES; 1.21K,1/16W,1%	R64
272431227576	TF041-TH-CAP;220uF,2.5V,+-20%	
796116040001	TF041-SPACER;H=5.0MM,M2X0.4P,	
796115040005	TF041-SPACER;H=3.0MM,M2.0X0.4	MTGH32,MTGH33
343114900045	TF041-SPACER;H=2MM,M3X0.5,ML9	MTGH7,MTGH8
271061333103	TF041-TH-RES;33K ,1/16W,1% ,	PR545,PR599
271061303103	TF041-TH-RES;30K ,1/16W,1% ,0	PR536,PR539,PR54,PR596
271071114104	TF041-TH-RES;110K,1/16W,1% 06	PR597
796116070006	TF041-SPRING;TCSBM46-6,IO GND	TP515,TP564,TP565
271061151110	TF041-TH-RES;150 ,1/16W, 1%,	R1000,R1001,R1005
288103315001	TF041-TL-DIODE ; ESD. V-PORT-	D4,D5,D8,D9
273030400088	TF041-TH;FERRITE BEAD 1000OHM	L14,L24,L522
288110150431	TF041-TH-TVS DIODE ; AZ1015-0	D10,D19,D21
273020100008	TF041-TH;Chip COMMON MODE CHO	L13,L16
272005105702	TF041-TH-CAP ;1U CR 50V +80-2	C146,C155,L9
273030200018	TF041-TH-FERRITE BEAD; 30OHM/	R564,R590,R602
272103220002	TF041-TH-CAP;2.2P,0.1P,25V,NP	C550,C564,C579

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Part Number	Description	Location(s)
288106830001	TF041-TH-TVS DIODE ; RSB6.8S-	
288100004002	TF041-TH-STEERING DIODE;USB00	U19,U20
288101515001	TF041-TL-DIODE ; ESD. V-PORT-	C502,C512,C515,C528
283480440006	TF041-TH-IC;EEPROM,AT24C02,2K	U7
288202301008	TF041-TH-TRANS;SI2301BDS,P-MO	PQ542,Q16,Q2000,Q25,Q37
796115070030	TF041- SPRING;M/B POGO-GND PA	TP566,TP567
797216403024	TF041-NUT;M3,HEX,FE,NIW	
796115040019	TF041-STANDOFF;H=5.2mm,M2.5*0	
796115050037	TF041-MYLAR;LAN,MODEM,M220	
796115060051	TF041-CR SPONGE;7LED-SHADING,	
797215202016	TF041-NUT;M2,HEX,SUS,PSV	
796115070001	TF041-TAFLON;CD-ROM,M220	
796115060018	TF041-RUBBER;DOCKING,POGO,M22	
796115050030	TF041-MYLAR;PCMCIA,M220	
796116000006	TF041-COPPER FOIL-MYLAR;M/B,M	
796115040020	TF041-STANDOFF;H=5.2mm,M2.5*0	
796115050082	TF041-SPACER;H=1,OUTER=3.7,IN	
797628422111	TF041-STANDOFF;H=11.0mm,M3*0.	
796115000066	TF041-CD ROM SLIDE ASSY,M220	
796114850034	TF041-MYLAR;DRAM,W130	
796116020002	TF041-BKT;1394B,M230	
412806000002	TF041-FAX MODEM 56K,RD02-D330	
796116060004	TF041-RUBBER;5*5*2T,M230	
796116060005	TF041-RUBBER;10*15*6.6T,M230	
796116060006	TF041-RUBBER;8*8*5.6T,M230	

Part Number	Description	Location(s)
796118270005	TF041-THERMAL PAD; ICS, A770;	
796116000007	TF041-CAP ASSY;2USB-1394,M230	
796115160011	TF041-GASKET; 733GT, A PART G	
796116070012	TF041-GASKET;733GT, LAN, USB	
323711900004	TF041-DRAM MODULE;DDR2 1G 533	
411116000013	TF041-TH-PWA; PWA-M230, CD-RO	
291000015058	TF041-TH-CON;HDR,MA,25P*2,.8M	J500
291000015059	TF041-TH-CON;HDR ,FM,25P*2,.8	J1
316116000002	TF041-TH-PCB;PWA-M230,CD-ROM	R00
796115040015	TF041-SPACER;H=2.5MM,02MM,M22	
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
226800020001	TF041-BOX;PET,1/20,SEC-V6,GPP	
221800020002	TF041-CARTON;425*310H240,SEC-	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	
523481614003	TF041-DVD COMBO DRIVE; UJ-DA7	
565111820002	TF041-S/W;NERO,RECORDER	
565111820003	TF041-S/W;POWERDVD,MEDIAMATIC	
796115100008	TF041-HOOK ASSY;DVD LOCK,M220	
338911120027	TF041-BATTERY PACK; LI, 11.1V	
242680600001	TF041-LABEL;BATT,11.1V/7.2AH,	
242683200024	TF041-LABEL;5*20,BLANK,COMMON	
242686000009	TF041-LABEL;LOT NUMBER,HOOK	
242687600004	TF041-LABEL;MIRRIR PAPER,WHIT	
335152000127	TF041-TH-FUSE;LR4-73X,POLY SW	
338937010065	TF041-BATTERY;LION,3.7V,2400m	

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Part Number	Description	Location(s)
342120100001	TF041-CONTACT PLATE;W5L58T0.1	
342120100002	TF041-CONTACT PLATE;W5L80T0.1	
342120100003	TF041-CONTACT PLATE;W5L11.5T0	
342680600001	TF041-CONTACT PLATE;W5L24T0.1	
342680600002	TF041-CONTACT PLATE;W5L45T0.1	
342686000017	TF041-TH-CONTACT PLATE;W4L30T	
342687600003	TF041-CONTACT PLATE;W5L9T0.13	
342687600005	TF041-CONTACT PLATE;W5L45T0.1	
344680600003	TF041-COVER;BATT,ML-900,PWR	
344680600004	TF041-HOUSING;BATT,ML-900,PWR	
346687600005	TF041-INSULATOR;ONE ROUND,FIB	
346801200001	TF041-INSULATOR;5,BATTERY ASS	
361400004013	TF041-ADHESIVE;ABS+PC PACK,G4	
411114300129	TF041-PWA;PWA-ML900/BATT GAUG	
331000005041	TF041-CON;BATTERY,FM,5P,5.0MM	
332100020023	TF041-WIRE;#20,UL1007,120MM,R	
332100020033	TF041-WIRE;#20,UL1007,22mm,BL	
332100020034	TF041-WIRE;#20,UL1007,22mm,RE	
332801500001	TF041-WIRE#26;UL1007,L18,BLUE	
332100026021	TF041-WIRE;#26,UL1007,152MM,B	
332110020189	TF041-WIRE;#20,UL1007,55MM,BL	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
411114300130	TF041-PWA;PWA-ML900/BATT GAUG	
271002391102	TF041-TH-RES;390,1/10W,1% ,08	R34
271046407105	TF041-TH-RES;0.040,2W,1%,2512	R9A1,R9B1,R9C1

Part Number	Description	Location(s)
271071100103	TF041-TH-RES;10 ,1/16W,1% ,	R7
271071101107	TF041-TH-RES;100 ,1/16W,1% ,	
271071104114	TF041-TH-RES;100K ,1/16W,.1%,	R13
271071104310	TF041-TH-RES;100K ,1/16W,5% ,	R12,R8
271071105312	TF041-TH-RES;1M ,1/16W,5% ,	R1,R18,R20,R3
271071471103	TF041-TH-RES;470 ,1/16W,1% ,	R30,R31,R32,R33
271071502304	TF041-TH-RES;5K ,1/16W,5% ,	R24,R5,R6
271071613101	TF041-TH-RES;61.9K,1/16W,1% ,	R10,R23
271071842101	TF041-TH-RES;8.45K,1/10W,1% ,	R22
272003474403	TF041-TH-CAP;.47U ,CR,25V,10%	C3
272003475401	TF041-TH-CAP;4.7U,25V,10%,080	C5
272005105402	TF041-TH-CAP;0.1U,CR,50V,10%,	C1,C2
272005220401	TF041-TH-CAP;.22U ,10% ,50V ,	C13,C14,C16,C21
272072474403	TF041-TH-CAP;0.47U,16V,10%,06	C12,C4,C9
272073104712	TF041-TH-CAP;0.1U,25V,10%,060	
272073105403	TF041-TH-CAP;1U, CR, 25V ,10%	C17
272075151309	TF041-TH-CAP;150P ,50V ,5% ,0	C11
272075222407	TF041-TH-CAP;2200P,50V ,10%,0	C7
272075680307	TF041-TH-CAP;68P ,50V ,5% ,0	C10,C6
286002084002	TF041-TH-IC;BQ2084,GAS GAUGE,	U1 V1.41
286029312002	TF041-TH-IC;BQ29312,PROTECTIO	U2
288100056026	TF041-TH-DIODE;UDZ5V6B-F,ZENE	ZD3,ZD4
288104148022	TF041-TH-DIODE;1N4148WS,75V,2	D1,D2
288204409003	TF041-TH-TRANS;AO4409,P-MOSFE	Q1,Q2,Q3,Q4
294112000001	TF041-TH-LED;GREEN,12-21SYGC/	LED2,LED3,LED4

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Part Number	Description	Location(s)
294112000002	TH041-TH-LED;RED,12-21SURC/S5	LED1
316683700021	TF041--PCB;PWA-ML900/BATT GAU	R0B
361200003064	TF041-SOLDER PASTE;SN96.5/AG3	
288100018007	TF041-TH-DIODE;PSD18C,TVS,18V	TVS2,TVS3
272001475412	TF041-TH-CAP;4.7U,10V,10%,080	C8
297040200023	TF041-TH-SW;PUSH BUTTON,DPDT,	SW
361200003201	TF041-ADHESIVE;SILICONE,DOW C	
242804400010	TF041-TH-LABEL;BAR CODE,20*5,	
288104024001	TF041-TH,DIODE,TVS ARRAY;40PF	TVS1
310111103049	TF041-THERMISTOR;10K,1%,RA,DI	RT1
332100026031	TF041-WIRE;#26,UL1007,115mm,Y	
335612000006	TF041-THERMAL CUTOFFS;378,8A/	
346671600025	TF041-INSULATOR;BATT ASSY,W7L	
335152000134	TF041-FUSE;THERMAL FUSE,G7F51	
342114300002	TF041-CONTACT PLATE;W5L20,ANG	
346114300017	TF041-INSULATOR;FIBRE,BATTERY	
346116000001	TF041-INSULATOR;L63W14mm,T=0.	
346116000002	TF041-INSULATOR;L60W26mm,T=0.	
346116000003	TF041-INSULATOR;L12W6mm,T=0.8	
225680620003	TF041-TAPE;ADHESIVE,DOUBLE-FA	
346685400025	TF041-INSULATOR;FIBRE,BATT,3	
346680800013	TF041-NYLON;BATTERY,PULL CLOT	
333025000015	TF041-SHRINK TUBE;300V,125,I.	
333020000039	TF041-SHRINK TUBE;600V,125'C,	
221680820005	TF041-CARTON;BATTERY,CAIMAN,P	

Part Number	Description	Location(s)
221680850002	TF041-PARTITION;BATTERY,MARLI	
221680850003	TF041-PARTITION;TOP/BTM,BATTE	
226687620001	TF041-SPONGE;320*290*10,CAIMA	
224801530001	TF041-PALLET;PLYWOOD,L1140*W1	
242679400008	TF041-LABEL;BAR CODE,NEW,COMM	
242686900045	TF041-LABEL;BLANK,55*25,OUTER	
225600020010	TF041-PE FILM;SKIN,PACKING	
225600020006	TF041-TAPE;CARTON,2.5W,30M/RL	
225600020002	TF041-TAPE;1/2",WRINKLE TAPE	
796115000025	TF041-GPS BOX;ASSY,M220	
796115070064	TF041-LABEL;110MM*85MM,PACKIN	
798961150005	TF041-CARTON;MAIN SYSTEM,M220	
798961150009	TF041-PE BAG;ANTI-STATIC,450*	
798961212013	TF041-PE BAG;ANTI-STATIC,210*	
796115070057	TF041-MYLAR;TRANSPARENT,320*2	
798961150012	TF041-END CAP;SYSTEM UNIT,14"	
798961150011	TF041-BOX;ACCESSORY KIT,14" &	
796116070010	TF041-LABEL;SAFETY/EMC/E-MARK	
796115000041	TF041-WLAN ANTENNA;ASSY,R,M22	
412116000006	TF041-PCB ASSY;MINIPCIE WLAN	
796115000042	TF041-WLAN ANTENNA;ASSY,L,M22	
796119072006	TF041-LABEL;INTEL CENTRINO DU	
791911151252	TF041-INT ASSY;(G)BLUETOOTH,M	
411116000037	TF041-TH-PWA;PWA-M230,BLUETOO	
291000021022	TF041-TH-CON;HDR,5P*2,MA,1.27	J3

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Part Number	Description	Location(s)
316116000012	TF041-TH-PCB;PWA-M230,BLUETOO	R00
272075102424	TF041-TH-CAP ;0.1U CR 50V 10%	C4
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1	C1,C2,C5
272071105412	TF041-TH-CAP;1U,10V,10%,0603,	C3
291000020611	TF041-TH-CON;HDR,MA,6P*1,1.25	J2
331840003017	TF041-TH-CON;MMCX,CONNECTOR,P	J1
271071241105	TF041-TH-RES;243,1/16W,1%,060	R2
271071151107	TF041-TH-RES;150 ,1/16W,1% ,	R1
271071103108	TF041-TH-RES;10K ,1/16W,1% ,	R5,R6,R8
286301117114	TF041-TH-IC;AMS1117,VOL REGUL	U1
412150000004	TF041-TH-PCB ASSY;BLUETOOTH M	U2
271071000312	TF041-TH-RES;0 ,1/16W,5% ,	R3
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
273000150374	TF041-TH-FERRITE CHIP;120OHM/	L1,L2,L3,L4,L5
361200003204	TF041-SOLDER PASTE;PF606-P;FO	
222672730002	TF041-PE BUBBLE BAG;BATTERY,2	
242600000566	TF041-LABEL;BLANK,7MM*7MM,PRC	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
411116000004	TF041-TH-PWA;PWA-M230,BLUETOO	
313002000097	TF041-TH-ANTENNA;BLUETOOHT,2.	X400
316116000001	TF041-TH-PCB;PWA-M230,BLUETOO	R00
242600000572	TF041-LABEL;4*3MM,HI-TEMP,260	
422116000005	TF041-CABLE ASSY;BLUETOOTH TO	P400
226683830101	TF041-CARTOON;L416,W269,FOR P	
222672730003	TF041-PE BUBBLE BAG;250*240mm	

Part Number	Description	Location(s)
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/C	
		P/N: 791901160015

11. Reference Material

❖ Intel Yonah CPU	Intel, INC
❖ Intel 945GM North Bridge	Intel, INC
❖ Intel ICH7-M South Bridge	Intel, INC
❖ Hitachi H8S/2140 KBC	Hitachi, INC
❖ M230 Hardware Engineering Specification	Technology Corp/MITAC
❖ Explode Views	Technology Corp/MITAC

SERVICE MANUAL FOR M230

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